RDECOM

TECHNICAL REPORT RDMR-WD-09-24

DESIGN, FABRICATION AND EVALUATION OF A MEMS-BASED,KA-BAND, 16-ELEMENT SUB-ARRAY

Janice C. Rock, Tracy D. Hudson
Weapons Development and Integration Directorate
Aviation and Missile Research, Development,
and Engineering Center

Brandon Wolfson, Daniel Lawrence
Phase IV Systems Operation
3405 Triana Boulevard
Huntsville, AL 35805

Brandon Pillans
Raytheon Space and Airborne Systems
Advanced Products Center
Dallas, TX 75243

Andrew R. Brown
A. Brown Design
46055 Bloomcrest Drive
Northville, MI 48167

Louis A. Coryell
CERDEC
Fort Monmouth, NJ 07703

Richard A. Milburn
Dynetics, Inc.
1002 Explorer Boulevard
Huntsville, AL 35806

November 2009

Aviation & Missile AMRDEC Strength Through Technology RD&E Center

DESTRUCTION NOTICE

FOR CLASSIFIED DOCUMENTS, FOLLOW THE PROCEDURES IN DoD 5200.22-M, INDUSTRIAL SECURITY MANUAL, SECTION II-19 OR DoD 5200.1-R, INFORMATION SECURITY PROGRAM REGULATION, CHAPTER IX. FOR UNCLASSIFIED, LIMITED DOCUMENTS, DESTROY BY ANY METHOD THAT WILL PREVENT DISCLOSURE OF CONTENTS OR RECONSTRUCTION OF THE DOCUMENT.

DISCLAIMER

THE FINDINGS IN THIS REPORT ARE NOT TO BE CONSTRUED AS AN OFFICIAL DEPARTMENT OF THE ARMY POSITION UNLESS SO DESIGNATED BY OTHER AUTHORIZED DOCUMENTS.

TRADE NAMES

USE OF TRADE NAMES OR MANUFACTURERS IN THIS REPORT DOES NOT CONSTITUTE AN OFFICIAL ENDORSEMENT OR APPROVAL OF THE USE OF SUCH COMMERCIAL HARDWARE OR SOFTWARE.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 074-0188

1. AGENCY USE ONLY	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	November 2009	Final

4. TITLE AND SUBTITLE
Design, Fabrication, and Evaluation of a MEMS-Based, Ka-band, 16-Element Sub-Array

5. FUNDING NUMBERS

6. AUTHOR(S)
Janice C. Rock, Tracy D. Hudson, Brandon Wolfson, Dan Lawrence, Brandon Pillans, Andy Brown, Louis Coryell, Richard Milburn

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Commander, U.S. Army Research, Development, and Engineering Command
ATTN: RDMR-WDG-R
Redstone Arsenal, AL 35898

8. PERFORMING ORGANIZATION REPORT NUMBER
TR-RDMR-WD-09-24

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE
A

13. ABSTRACT ***(Maximum 200 Words)***

The Aviation and Missile Research, Development and Engineering Center (AMRDEC) has recently completed an Army Technology Objective (ATO) aimed at furthering phased arrays for both tactical seekers and communication links. The ATO has been pursuing both MicroElectroMechanical Systems (MEMS) and Monolithic Microwave Integrated Circuit (MMIC)-based phase shifters with an overall goal of reducing missile seeker costs by 50 percent based on the missile mission.

In a collaborative effort with the Communications-Electronics Research, Development and Engineering Center (CERDEC), the AMRDEC has worked to improve the maturity of Radio Frequency (RF) MEMS devices for use in phase shifters for phased arrays.

(continued on page iii)

14. SUBJECT TERMS
Phased Arrays, Electronically-Steerable Phased Arrays, Integration, MEMS

15. NUMBER OF PAGES
54

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	SAR

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. Z39-18
298-102

ABSTRACT (CONTINUED)

This report will demonstrate that RF MEMS have vastly improved in reliability over the past few years. Additionally, background information and most current results of a task to implement a 16-element phased sub-array with RF MEMS-based phase shifters will be presented. The slat will be centered at 33.4GHz and will utilize one-half wavelength spacing between elements. The individual elements will consist of Vivaldi antennas. Taylor Weighting will be applied to lower the overall sidelobes.

This report will discuss the MEMS design being produced including the current maturity of the design, insertion loss, power consumption, linearity and reliability of the phasing network.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS

LIST OF TABLES

I. INTRODUCTION AND BACKGROUND

In 2006, the Communications-Electronics Research, Development and Engineering Center (CERDEC) issued a Broad Agency Announcement (BAA) requesting proposals for Affordable Radio Frequency (RF) Micro Electro-Mechanical Switch (MEMS) Phase Shifters for Phased Arrays Manufacturing Technology Objective (APSPA MEMS) Program. The objective was to develop a volume production facility for reliable, low-cost MEMS phased shifters for use in phased arrays for both active and passive missile seekers and for on-the-move Satellite Command (SATCOM) communications systems for the Warfighter. Aviation and Missile Research, Development, and Engineering Center (AMRDEC) has been involved in this program since its inception and, in 2008, initiated an effort to demonstrate the results of the CERDEC Manufacturing Technology Objective (MTO) program in a 16-element, Ka-band, MEMS-based electronically-steerable slat.

A major contributor to both the cost and loss of these systems, particularly in the passive systems, is the packaged Monolithic Microwave Integrated Circuit (MMIC) phase shifter. MEMS phase shifters offer a low-cost (<$10), low-loss alternative to these components. The successful completion of this ManTech program should result in an overall cost reduction of up to 25 percent for phased array antennas operating in the Ku, K, and Ka frequency bands. In addition, MEMS-based phase shifting promises to reduce the loss by one-half to two-thirds compared to MMIC-based phase shifting.

The prime contractor, Raytheon Space and Airborne Systems, has produced a 4-bit packaged phase shifter demonstrating approximately 1.7 to 3.0 dB of loss. The switch and phase shifter design will be discussed in this report.

II. SWITCH DESIGN

In 1995, Raytheon pioneered the development of RF MEMS technology for microwave and millimeter-wave applications with the development of the first capacitive RF switch [1]. Since then, Raytheon has been involved in the design and development of high-performance RF MEMS for advanced phased-array applications. Raytheon has developed an RF MEMS switch that is optimized for low RF insertion loss, high switching speed, high-power handling, excellent temperature stability, and long cycle lifetime (Table 1). With support from the Army, Defense Army Research Projects Agency (DARPA), the Office of Naval Research (ONR), and Air Force Research Laboratory (AFRL), Raytheon has demonstrated low-loss, multi-bit phase shifters, routers, and digitally tunable filters across the entire 0.1 to 50 GHz frequency range. A picture of the basic switch is shown in Figure 1.

Table 1. RF MEMS Switch Performance Summary

RF MEMS Switch Performance	
Insertion loss at 40 GHz	<0.07 dB
Isolation at 40 GHz	>25 dB
Temp Stability	-55°C to +85°C
Switching speed	<5 μs
Intercept point	>+87 dBm
Switching voltage	30 volts
Reliability	$> 10^{11}$ cycles
Size	280 × 120 μm
Power Consumption	<1μW

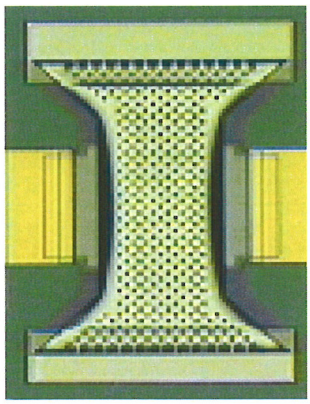


Figure 1. Top-view of the Individual RF MEMS Switch

Raytheon's latest switch design achieves over 200 billion operating cycles without failure with a switching speed under 5 microseconds and power consumption under 1 microwatt. Innovations in switch membrane materials and device structure now provide much greater thermal stability, and prototype switches operate from -55 °C through +85 °C with actuation voltage variance of only a few volts.

Typical switch insertion loss is less than 0.1 dB at frequencies through 40 GHz. These switches are constructed using only metals and dielectrics, and detailed measurements of Raytheon's RF MEMS switches show no observable RF nonlinearity to intercept points as high as +87 dBm (5,000 watts) [2].

A. Packaging

Like all micromechanical systems, RF MEMS switches are subject to damage from corrosion and contamination from exposure to dust, air, and moisture. Encapsulating the switches in a particle-free, hermetic package eliminates failures due to these environmental effects. To meet operational requirements, the package must be compact and not degrade RF circuit performance. The challenge is to provide this protection at very low cost in a high volume production environment. Over the last three years, Raytheon has developed a highly innovative wafer-level hermetic packaging approach [3] that meets all requirements for reliability, operating temperature range, yield, and cost. This near-hermetic package (Fig. 2) adds very little to the total circuit price.

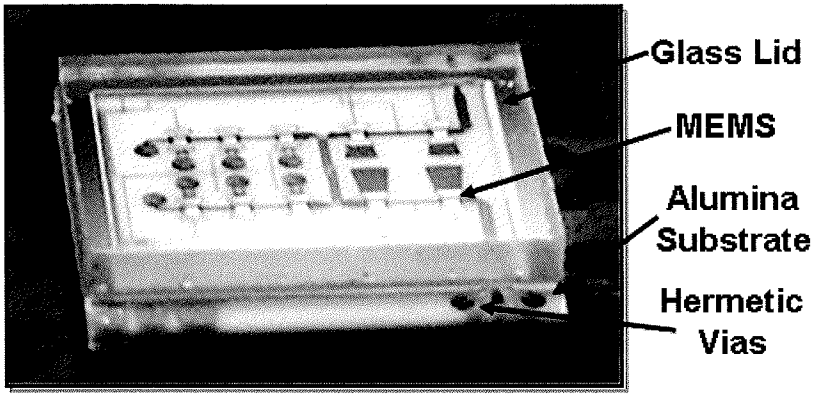


Figure 2. Photograph of Near-Hermetic Wafer-Scale Packaged RF MEMS

B. Maturity

Under the Army's APSPA MEMS Program, Raytheon is currently fabricating RF MEMS phase shifters [4] in its Advanced Multilayer Interconnect (AMI) facility, an ISO 9001-qualified manufacturing environment that has fabricated more than 500,000 comparable circuits. The APSPA Mantech program is a three-year, $5M effort aimed at raising the technology and manufacturing readiness levels of Raytheon's RF MEMS technology to eight for system insertion. The program is currently in its third year with much success. Included in this effort are improvements in reliability (10^{12}), RF power handling (2W hot), operating temperature range (-55 to +85 °C), switching speed (<5μs), and cost. By leveraging the Army's RF MEMS Mantech program investment, Raytheon is able to provide low-loss, highly reliable switches for many applications including low-cost phased arrays.

III. PHASE SHIFTER DESIGN

The phase shifter design is based on a class II loaded-line topology [5, 6]. This topology was a compromise of simplicity, low-loss, compact size, and fit well with the equivalent model of the MEMS switch. The class II loaded line consists of a pi-network of a switched shunt reactance, a series transmission line of length L1_eff, and impedance Z1_eff as shown in Figure 3. Full theory and design examples of this concept is well documented in Reference [5] and not detailed here. For the implementation used in this system, the switched reactance consists of the MEMS switch followed by a shunt radial stub [7]. The zero state consists of reactive loading of the switch up-state followed by the radial stub. The phase shifted state uses the down state switch capacitance and the radial stub. One of the major difficulties with a loaded line topology is obtaining large phase shifts while maintaining bandwidth. Typically, 45 degrees is the largest state implemented with a loaded-line topology [6]. Higher phase shifts are typically done by cascading 45-degree sections. However, even the 45-degree stage proved difficult to implement and meet bandwidth requirements with the required loaded line and the Con/Coff ratio at Ka-band. Therefore, even multiple stages were used for the 45-degree bit. To further reduce the number of stages required in cascaded bits, ripple was introduced. For the 90- and 180-degree stages, the phase shift per section and overall impedance values were adjusted to provide equal ripple response. This has the effect of allowing one to reduce the number of cascaded sections while still maintaining bandwidth when two or more stages are used, thus allowing the 90-degree stage to be implemented with as few as two sections and the 180-degree with only four stages. However, the out-of-band performance of these stages rolls off much faster than conventional cascaded sections.

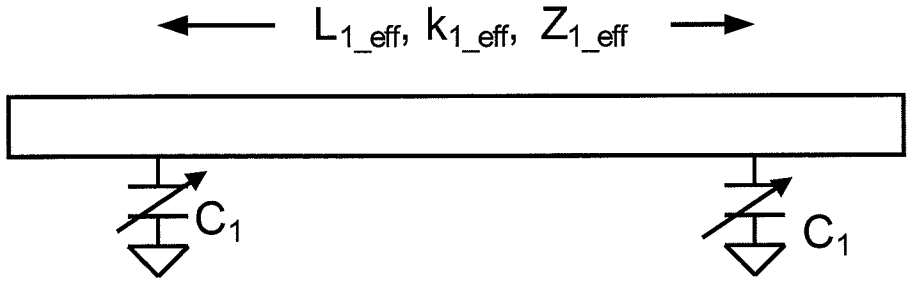


Figure 3. Topology of a Capacitively Loaded Class II Loaded-Line Phase Shifter

The package is based on a hermetic wafer scale package 20mm^2 exterior dimensions. In addition to having to meander the phase shifter through the package interior, the transitions in and out of the package required optimization for this band of operation. Due to the high capacitance of the feedthrough line to the grounded seal ring, the feeds were made very inductive to attempt to tune out some of the shunt capacitance. An optimization was performed to minimize in-band insertion loss from the package transition. Figure 4 shows the resulting, packaged phase shifter. Measurements of isolated package transitions show < 0.2 dB insertion loss.

The fabricated and packaged phase shifters were measured. All data shown is from an average, fully packaged phase shifter with no de-embedding performed. There was a slight shift in performance from the designed values, primarily shown in the 22.5- and 45-degree bits. Both of these bits show excessive phase shift compared to the designed values. This can be fixed in future designs and is not a limitation of the technology. Even with the long 22.5- and 45-degree states, the Root-Mean-Square (RMS) phase error at 33 GHz is only 8.8 degrees. The total insertion loss at 33 GHz is 2.5 dB average with an RMS amplitude error of 0.3 dB. Even though the RMS phase error is high, primarily due to the 22.5- and 45-degrees, the presented phase shifter shows vastly reduced insertion loss compared with other MMIC technologies such as the Triquint TGP2102 5-bit phase shifter (7 dB nominal insertion loss). The results of the laboratory evaluation are presented in Figures 5 through 7.

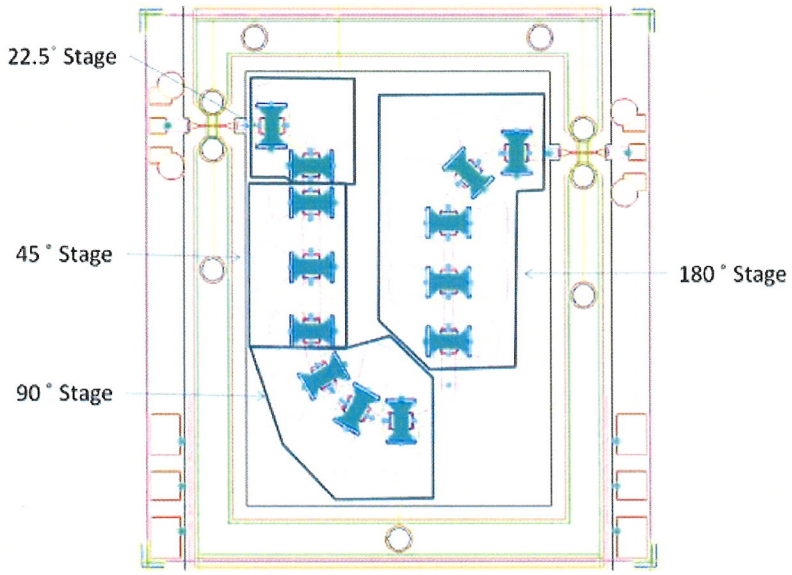


Figure 4. Layout of the Ka-Band Phase Shifter

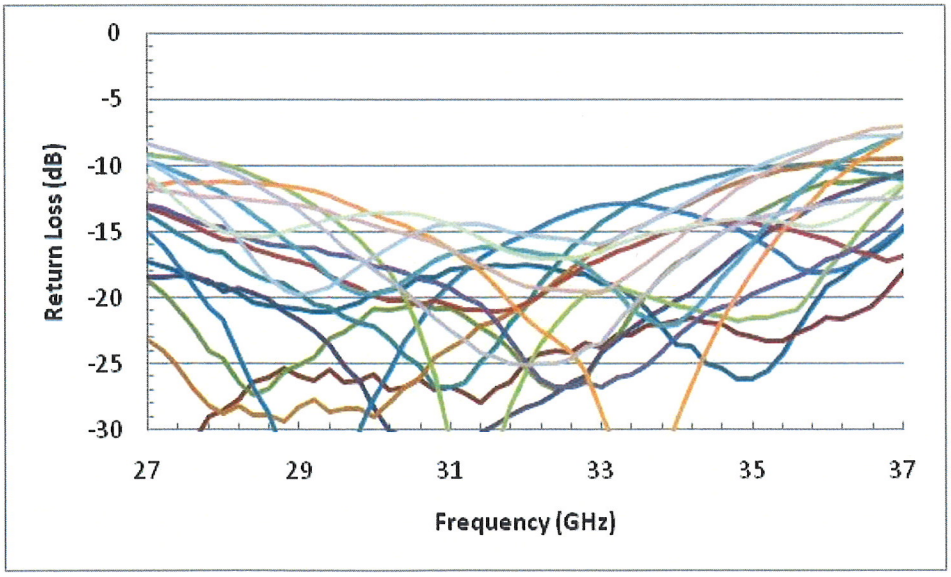


Figure 5. Measured Return Loss

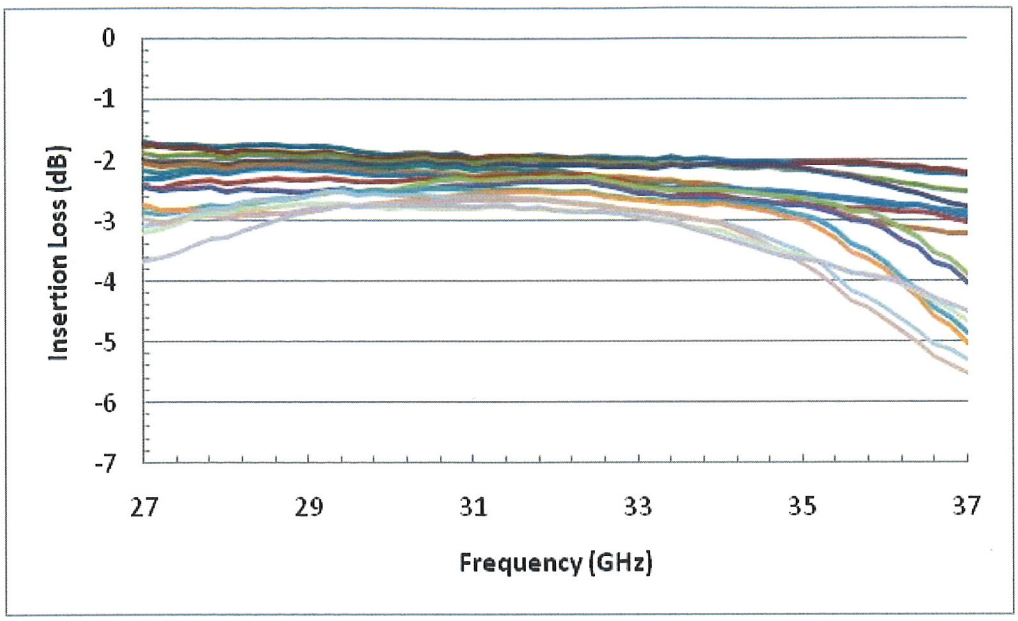


Figure 6. Measured Insertion Loss of all 16 States

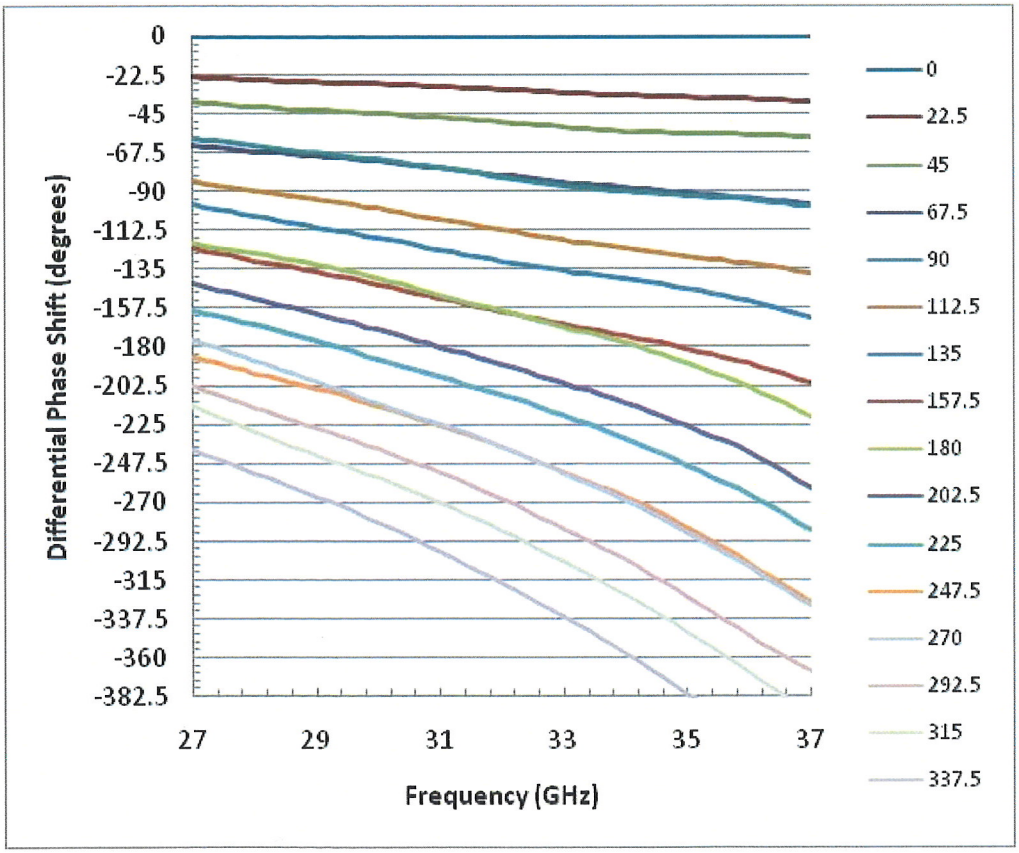


Figure 7. Measured Phase Shift

IV. PHASED ARRAY T/R ASSEMBLY

The slat assembly is composed of the microwave antenna slat subassembly mated to a control and interface subassembly. A block diagram of the slat assembly is shown in Figure 8. The microwave antenna slat subassembly contains all of the assembly's microwave circuitry, as well as the circuitry necessary to support the operation of the microwave devices, such as DC regulators, power sequencing circuits, switch drivers and high-voltage multiplexors. The high-voltage multiplexors are used to deliver the high-voltage control signals, necessary to actuate the MEMS switches in the phase shifters, to the appropriate inputs of the MEMS phase shifters. The control and interface subassembly provides the user with a simple method of controlling and interfacing with the microwave antenna slat subassembly.

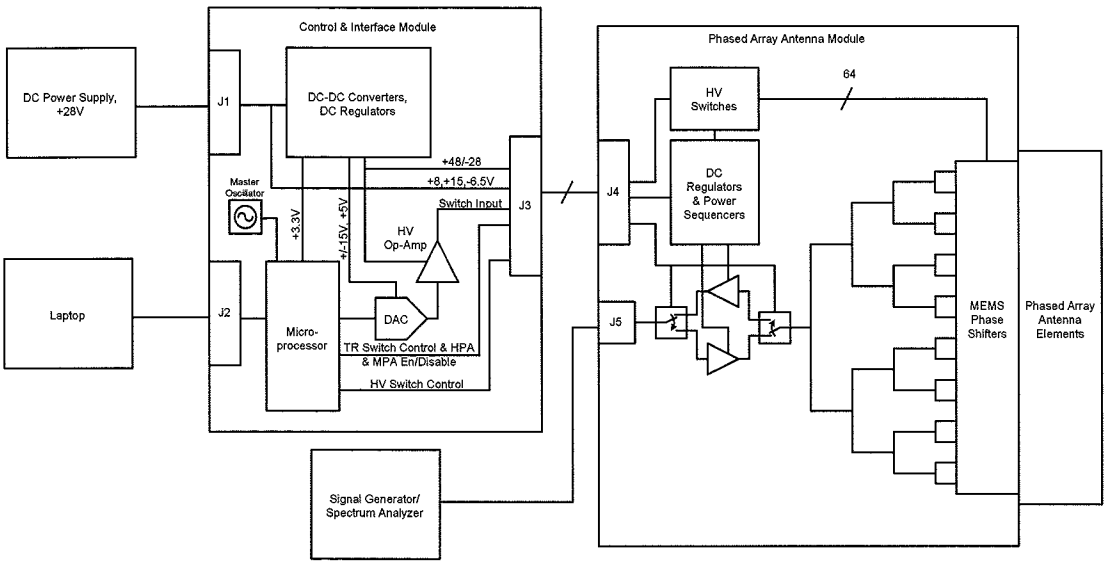


Figure 8. Block Diagram of Antenna Slat Assembly

A. Microwave Antenna Slat Subassembly

The microwave antenna slat subassembly implements 16 Vivaldi antennas and a 16-way 20dB Taylor weighted power divider to drive the MEMS phase shifters at the inputs to the antennas. A transmit/receive circuit made up of Ka-band MMIC amplifiers and switches is utilized at the input of the power divider to boost the received signals. The Vivaldi antenna was chosen for its broadband performance and ease of implementation in a microstrip printed circuit design. The antenna design was finalized and its performance simulated using High Frequency Structure Simulation (HFSS) Three-Dimensional (3-D) electromagnetic modeling software. The 16-way power divider implements the 20dB Taylor weights by cascading unequal power dividers. The design of the power divider was completed and modeled using Microwave Office simulation and design software. The circuits used to control the operational states of the TX/RX circuitry, as well as the phase states of the 16 MEMS phase shifters, are located on the backside of the multilayer board used to implement the microwave circuitry. These circuits on the backside of the microwave antenna subassembly are controlled by signals output from the control and interface subassembly.

B. Antenna Design

Vivaldi antennas were first introduced as a new class of frequency independent antennas that produce a travelling-wave through an exponentially tapered slot [8]. These types of antenna are commonly referred to as Tapered Slot Antennas (TSA) with many possible variations on the length and profile of the taper. A modified TSA, known as the antipodal Vivaldi antenna, was introduced later with the benefit of direct feeding by a microstrip line [9]. The antipodal Vivaldi antenna element design provides a wideband, broad radiation pattern that is well-suited for use in a phased array antenna. Another attractive feature of the Vivaldi antenna is the ease with which it can be driven with a microstrip feed network, and thus, integrated with surface-mount phase shifter components [10]. The basic radiating element is shown in Figure 9. The element is fabricated from a single substrate layer with metallization on both sides. A profile of the substrate (5 mil thickness, $\varepsilon_r = 3.0$) is shown in Figure 10. The element begins by exponentially tapering the ground plane of the microstrip feed line until the width is the same as the signal line. For a good impedance match, the taper extends for about 1 wavelength. At this point the ground plane and signal lines are flared symmetrically on opposite sides of the substrate to form a broadband dipole radiator. Tuning of the antenna is achieved by empirical adjustment of the flare geometry.

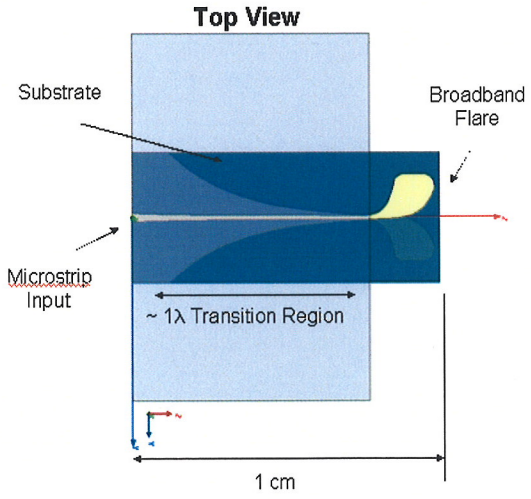


Figure 9. Antipodal Vivaldi Element Design

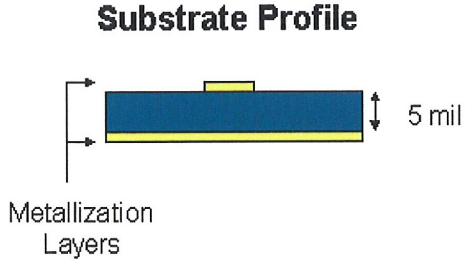


Figure 10. Substrate Profile

C. Antenna Modeling and Simulation

A four-element subarray of Vivaldi antennas is shown in Figure 11. An HFSS simulation of the four-element subarray has been constructed in order to tune the radiating elements in the array environment. The overall size of the simulated array has been kept small to maintain reasonable run-times. Results in Figure 12 show the input match for each element in the subarray. Notice the return loss is better than 10 dB across the complete bandwidth, confirming the broadband nature of the Vivaldi elements as shown in Figure 12. Slight variations in the resonance of each element can be attributed to the mutual coupling and parasitic loading of different elements in the array. Scanning of the subarray in the E-plane is accomplished by applying a progressive phase shift across the array. HFSS simulation results showing the array radiation pattern for several scan angles are shown in Figure13. Uniform amplitude weighting was used for the subarray simulation. Note that scanning past 45 degree results in increased sidelobes and a reduced mainlobe due to the roll-off of the element pattern.

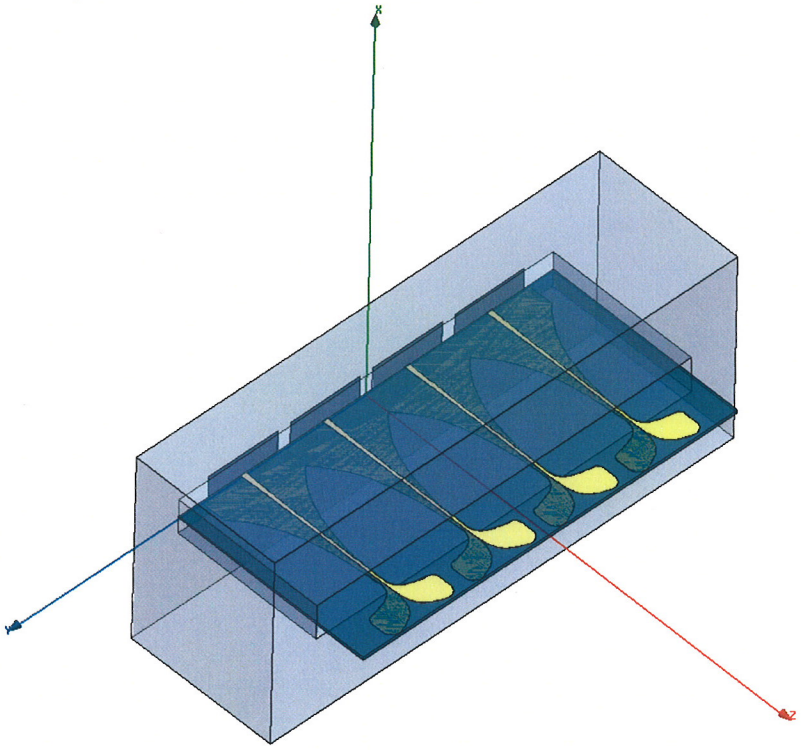


Figure 11. Four-Element Subarray HFSS Model

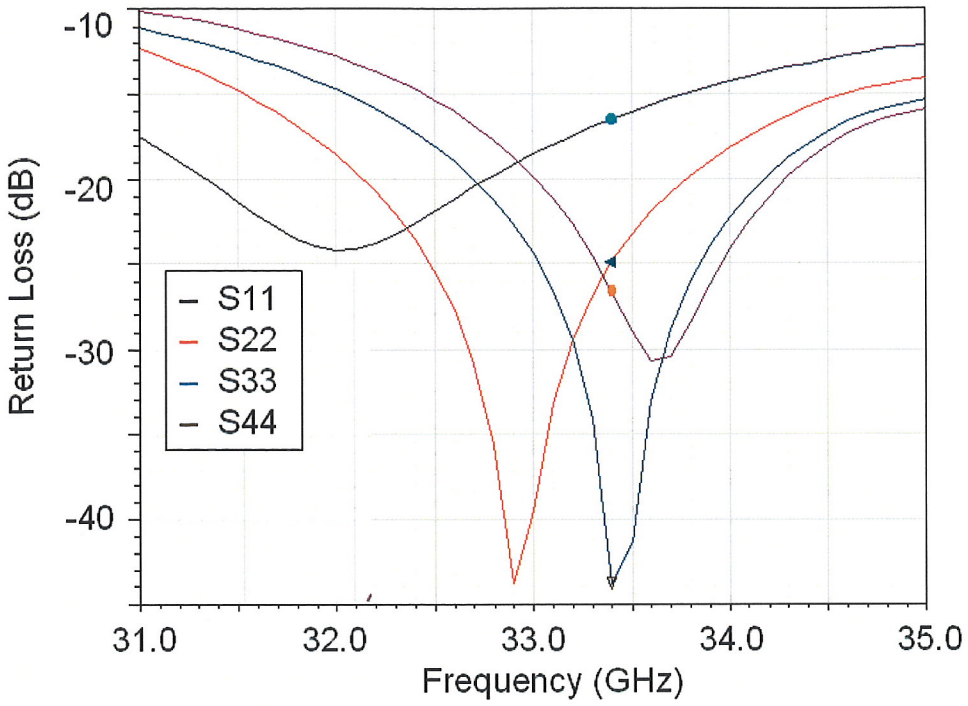


Figure 12. Input Match for Each Element in the Four-Element Subarray

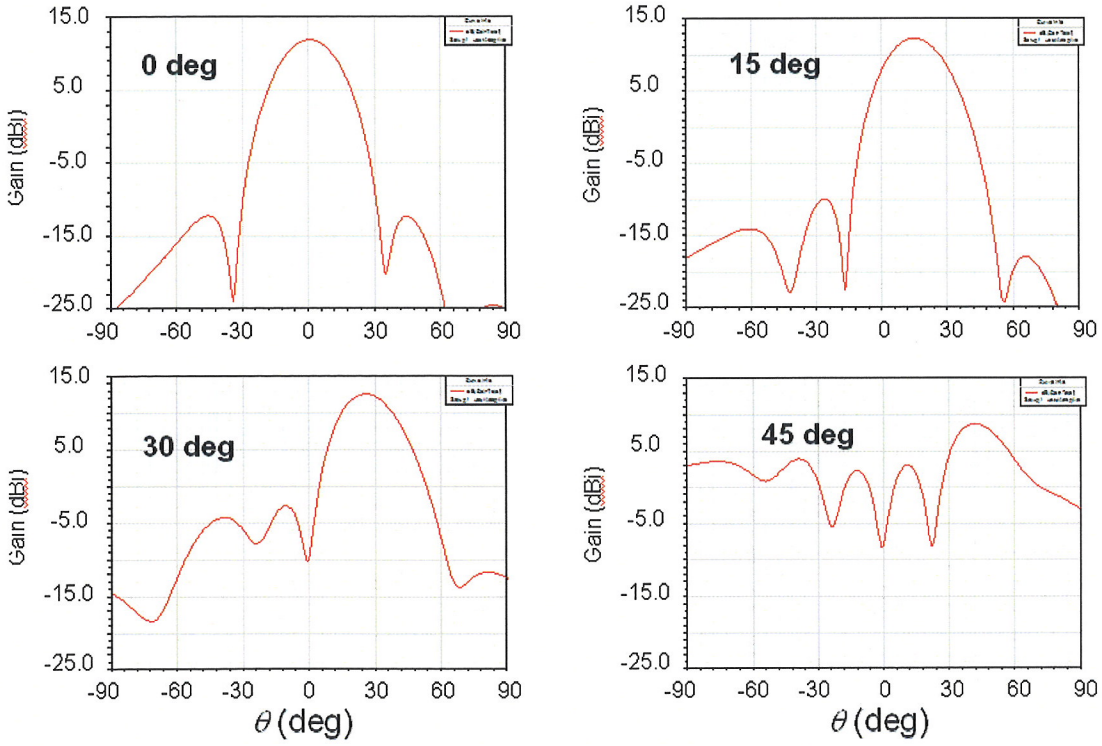


Figure 13. Scanned E-plane Radiation Patterns for the Four-Element Subarray

D. Power Divider

The 16-way power divider is constructed from 4 stages of 2-way power dividers. The first three stages are made by simple T-junction power dividers, and the final stage of power divider utilize unequal split Wilkinson power dividers. The use of T-junction power dividers for the first three stages was done to reduce design complexity and space and to eliminate the need for isolation resistors. While the T-junction power dividers simplify the design, they do not provide isolation between the output ports. It was found that the performance of the power divider could be significantly degraded if its 16 outputs were not terminated with a load that was well matched ($\Gamma \leq$-20dB) to the design impedance of 50 ohms. In some cases the MEMS phase shifters have been shown to have an input return loss as high as -15dB to -10dB in the band of interest, which was still not good enough to prevent performance degradation of the power divider (Fig. 5). Along these same lines, the input return loss of the MEMS phase shifters can vary with changing phase shift settings causing varying performance degradation of the power divider (Fig. 6). For these reasons the final stage of the power divider was chosen to be Wilkinson power dividers. This provided enough port-to-port isolation to allow for the imperfect loads presented by the MEMS phase shifters.

For the design of the power divider 20dB Taylor one-parameter weighting was used. The value of 20dB was chosen to provide some reduction in sidelobe level while making the design of the power divider more feasible. The Taylor weighting coefficients can be found from Equations (1) and (2) below.

$$w_n = \frac{J_0\left(j\pi\beta\sqrt{1-\left(2\frac{n-\frac{N-1}{2}}{N-1}\right)^2}\right)}{J_0(j\pi\beta)} \tag{1}$$

J_0 is the modified Bessel function and β is related to the Side Lobe Level (SLL) and can be found by finding the root of Equation (2). In Equation (2) SLL is the desired level measured in dB.

$$\beta = 10^{\frac{SLL}{10}} - 4.603\frac{\sinh(\pi\beta)}{\pi\beta} \tag{2}$$

The relative output powers at the two output ports of a two-way power divider can be defined as shown in Equation (3). P_1 and P_2 are the relative output powers at ports 1 and 2 relative to P_{in}.

$$\begin{aligned} P_1 &= \alpha P_{in} \\ P_2 &= (1-\alpha)P_{in} \end{aligned} \quad where \quad 0<\alpha<1 \tag{3}$$

Once the Taylor weighting coefficients are known, one can find the values of α in Equation (3) for each of the power dividers. Since we have an even number of outputs and the Taylor weighting coefficients are symmetric, the value of α for the first stage power divider will always be 0.5 and the values of α for the cascaded power dividers at each output of the first power divider will simply be mirrored copies of each other. For this design the values of α at each stage are shown in Table 2.

Table 2. Values of α for Each Power Divider Stage

Stage	**α value**							
1	0.5							
2	0.2633				0.2633			
3	0.283		0.438		0.438		0.283	
4	0.3495	0.4111	0.4516	0.4846	0.4846	0.4516	0.4111	0.3495

For a simple T-junction power divider one can use the values of α above to find the necessary impedance that needs to be presented to the power divider input port by each of the two output ports to get the desired unequal power division. The relationship between the impedances at each side of the T-junction to the values of α is shown in Equation (4).

$$Z_1 = \frac{Z_0}{\alpha}$$
$$Z_2 = \frac{Z_0}{(1-\alpha)} \tag{4}$$

In Equation (4) Z_1 and Z_2 are the impedances presented to each side of the T-junction power divider and Z_0 is the characteristic impedance of the input to the T-junction as depicted in Figure 14 where the second stage T-junction power divider is shown. One quickly finds that the greater the sidelobe reduction the more difficult it becomes to design some of the power dividers due to the unreasonably high values of impedance needed. The high impedances can become an issue when they lead to trace widths that are too narrow for standard fabrication processes. The large ratio between the two output impedances also makes the design less trivial since one side of the T-junction will require a relatively wide trace while the other side requires relatively very narrow trace. This is the main reason why 20dB Taylor weights were chosen over those with more sidelobe level reduction. The need for unreasonably narrow traces can be alleviated by decreasing the value of Z_0 at the input to each power divider stage. The approach taken for this design is shown in Figures 14 and 15. Figure 15 shows the overall 16-way 20dB Taylor weighted power divider design. It can be seen that the final stage of power dividers are Wilkinson power dividers. As mentioned previously, this was done to provide some channel-to-channel isolation to help prevent performance degradation due to the imperfect impedance match presented by the MEMS phase shifters that are fed by this power divider.

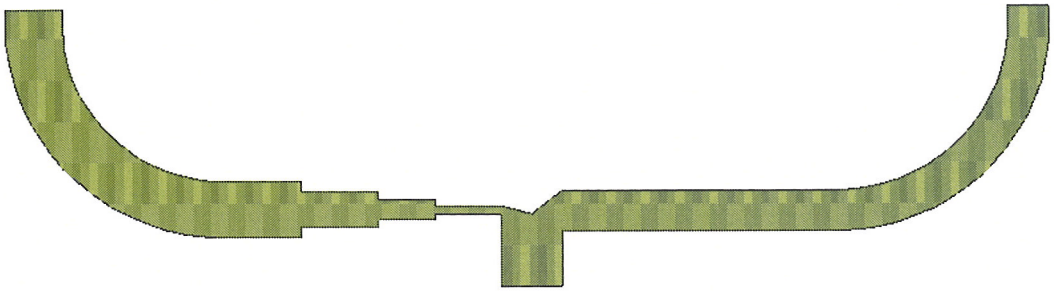


Figure 14. Second Stage Two-way T-junction Power Divider

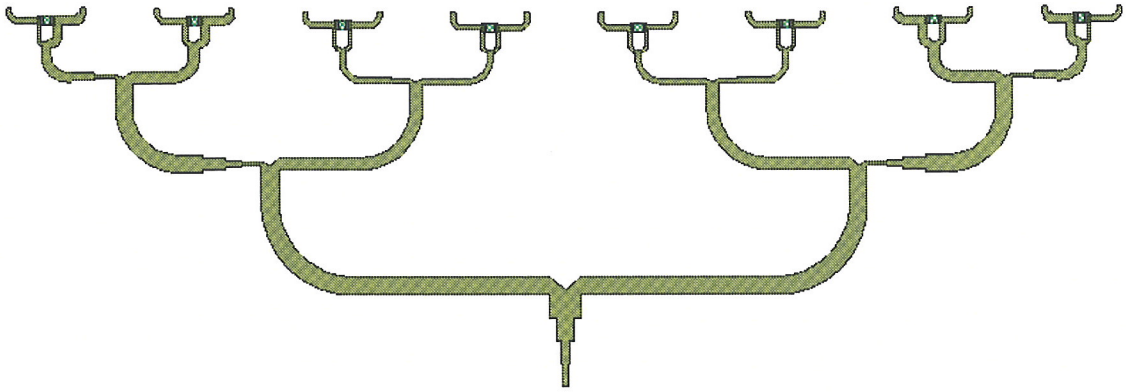


Figure 15. 16-way Taylor Weighted Power Divider

E. Modeling and Simulation

The modeling and simulation for the power divider was completed in Microwave Office. The substrate used is the same as that used for the antenna design (5 mil thickness, ε_r = 3.0). It can be seen from Figure 15 that the input characteristic impedances for each stage were chosen strategically to both keep the narrower line widths in the design as a reasonable width, as well as remove the need for impedance transformers on one side of many of the power dividers.

Figure 16 shows the insertion loss and the return loss from the input of the power divider to either of the two center-most output ports. Here it is seen that the power divider is well matched over the entire band of interest. The expected insertion loss for the two center ports is -9.72dB in a lossless system.

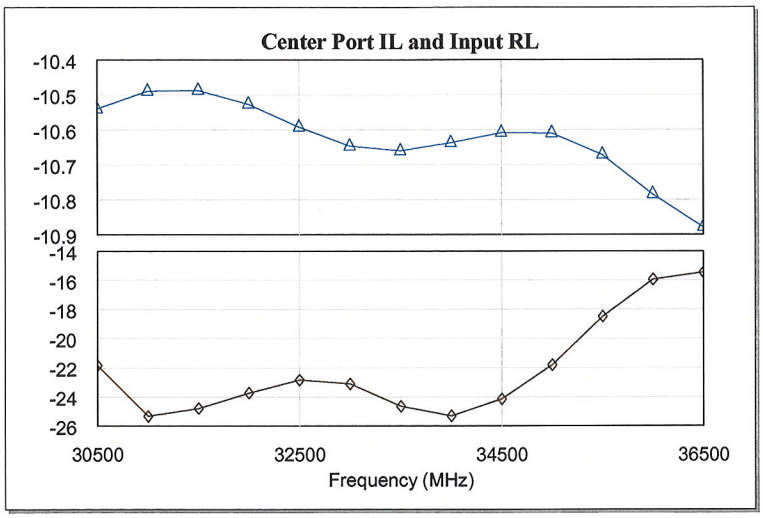


Figure 16. Simulation Results for the Input Loss

From the simulation it is seen that the circuit has an approximate substrate loss of 1dB, which is to be expected at these frequencies. For the rest of the ports it is best to look at the output power relative to the center-most ports to ensure the design effectively implements the desired Taylor weighting. Figure 17 shows this by plotting the difference between the power at the center port and the adjacent ports. In this figure, the markers are placed at the center of the band of interest and the insertion loss of each port relative to the center port insertion loss of Figure 16 is shown. The values at each marker are shown in the legend. The marker m1 represents the port farthest from the center, whereas m7 represents the port nearest the center port. Since the design is symmetrical, we only need to look at one side of the design.

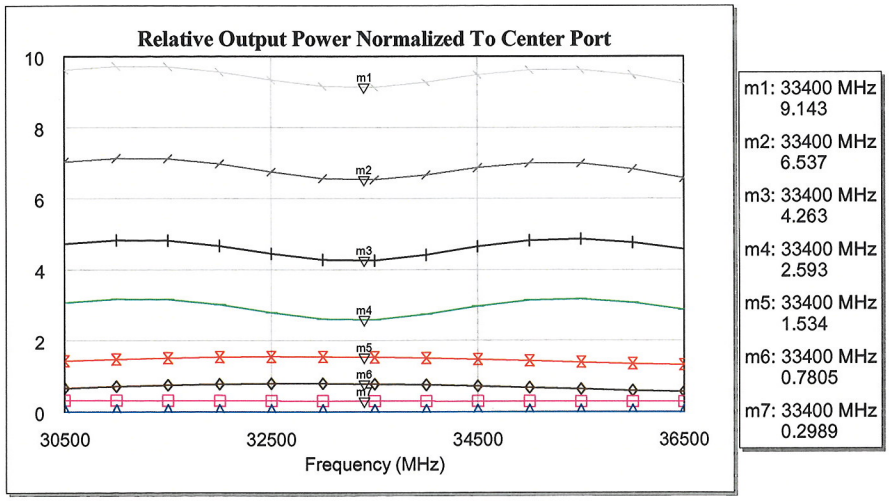


Figure 17. Plot of the Difference Between the Power at the Center and Adjacent Ports

The expected relative output powers at each port can be found using the Taylor weight coefficients. These are shown in Table 3 along with the simulated values shown in Figure 17. In the Table 3, port numbers 1 through 7 are synonymous to markers m1-7 in Figure 17 and likewise represent going from the outermost port to the inner most. In this table it is seen that the calculated and measured values are closely matched.

Table 3. Output Parameter Difference as Measured from Center Port to Referenced Port

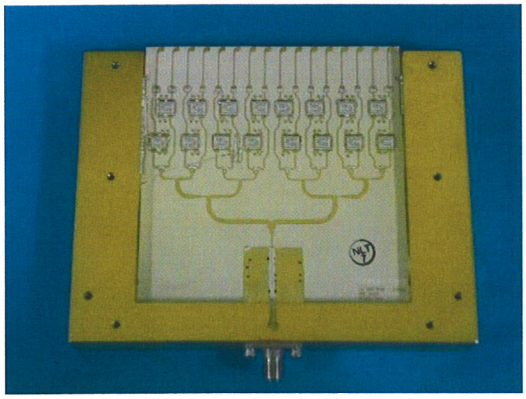
Port #	Calculated	Simulated
1	9.13	9.143
2	6.44	6.537
3	4.39	4.263
4	2.83	2.593
5	1.66	1.534
6	0.81	0.7805
7	0.27	0.2989

F. Module Layout and Controller Design

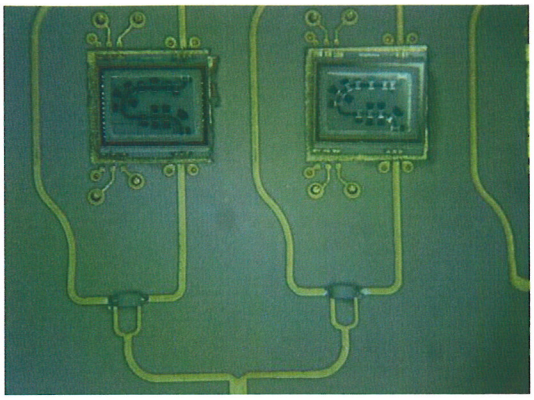
The MEMS Phased Array Assembly is made up of the Microwave Antenna Subassembly mated to the Control and Interface Subassembly. The division of the MEMS Phased Array Assembly was done strategically to provide a path forward for future developments where it may be desired to design a Two-Dimensional (2-D) array. The circuit design of the Control and Interface Subassembly could supply the appropriate signals and voltages to multiple antenna array slats. The architecture of the Microwave Antenna Subassembly would require mostly mechanical upgrades to account for the height restrictions that would be created by stacking multiple slats to form the 2-D array. The designs of each of the two subassemblies will be discussed in more detail here.

G. Microwave Subassembly Design

The microwave substrate used for fabricating the phased array antenna was designed to also provide the microstrip transmission lines that distribute the microwave signals between active components in the array. A 0.005-inch thick Rogers RO3003 substrate was used for this application. The substrate was designed with cutouts for each of the active components, as well as the MEMS phase shifters. The design of the RF assembly allowed for microwave coplanar probing of each phase shifter output. This was accomplished by placing two small RF probe boards between the output of each phase shifter and input to the corresponding Vivaldi element. The microwave probe boards are 0.050-inch long pieces of 0.005-inch thick alumina microstrip having ground pads at one end of the substrate in order to accommodate a Ground-Signal-Ground (GSG) microwave probe. The microstrip and ground pads were spaced for a probe pitch of 150 micrometers. One probe board allowed for phase measurement between the phase shifter with respect to the common microwave input connector. Figure 18 shows a picture of the microwave board assembly. The initial plan was to populate an amplified transceiver section at the input of the 16-way power divider. Due to cost and schedule restraints, the decision was made to move forward with the fully passive array in order to achieve the primary goal of demonstrating the ability to steer a beam using the MEMS phase shifters. The empty spot on the lower end of the microwave substrate is the area where the transceiver circuitry could be placed.



Microwave Circuitry



Power Divider and Phase Shifters

Figure 18. Phased Array Assembly, RF Substrate and MEMS Phase Shifters

In the Microwave Antenna Subassembly on the opposite side of the microwave substrate is the microwave module interface board. This board receives the voltages and control signals from the Control and Interface Subassembly. The voltages are used to supply power to amplifiers, as well as the high voltage switches required to control the MEMS phase shifters. The control signals are mainly used to command the high-voltage switches to assert the provided high- voltage control to the desired MEMS phase shifter inputs. A picture of the microwave module interface board is shown in Figure 19.

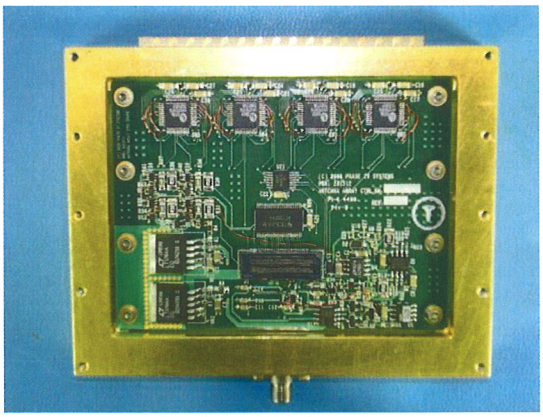
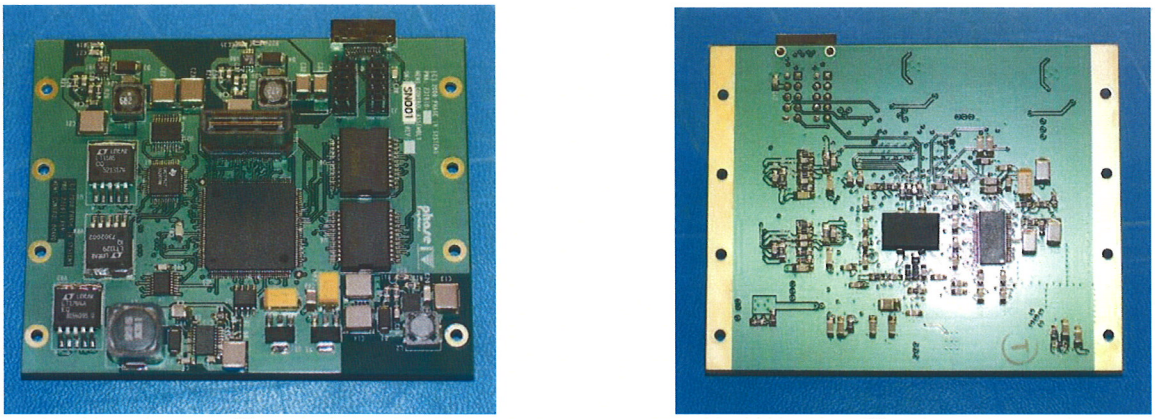


Figure 19. Microwave Module Interface Board

H. Control and Interface Subassembly

The control and interface subassembly houses the circuitry necessary to provide the control signals and various voltages to the Microwave Antenna Subassembly. The Control and Interface Subassembly also provides a means to communicate with the phased array assembly using a standard computer interface. The circuitry mainly consists of a Field Programmable Gate Array (FPGA), a Digital-to-Analog Converter (DAC), high-voltage op-amps, and DC-DC converters. A Graphical User Interface was developed to interface with the FPGA and provide the user with a method to control the various states of the phased array module. The FPGA is also used to control the DAC whose output is buffered and amplified to the high-voltage levels needed to drive the MEMS phase shifters. This buffering and amplification is done by high-voltage op-amps. The outputs of the op-amps are presented to the Microwave Antenna Subassembly via the microwave module interface board. As mentioned earlier, the microwave module interface board then provides these op-amp outputs to the high-voltage switches to set the appropriate bits of the MEMS phase shifters and ultimately steer the antenna array beam pattern. The DC-DC converters allow the phased array assembly to be powered by a single 28-Volt source. Figures 20 and 21 show pictures of the two sides of the control and interface board, as well as the control and interface board mounted in the control and interface subassembly.



Top *Bottom*

Figure 20. Control and Interface Board, Top and Bottom

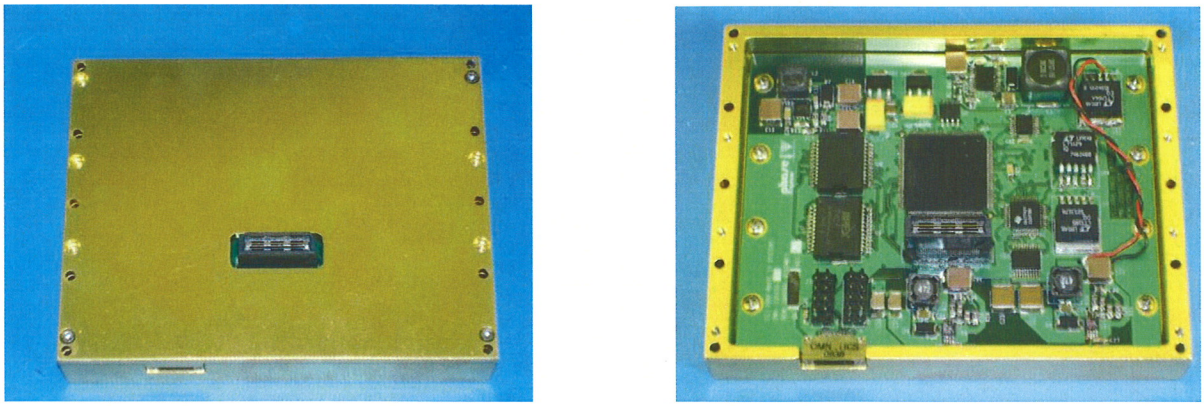


Figure 21. Control and Interface Subassembly With the Lid On and Off

I. Computer User Interface

A computer user interface was developed using Visual C++. A screen shot of the Phased Array Interface (PAI) is shown in Figure 22. The MEMS Phased Array Assembly can e controlled simply by connecting to the RS232 serial port present on the back of most PCs. The load text button is used to load a look-up table of phase shifter settings. The phase shifter settings are then asserted by choosing the desired beam steer angle using the slider bar and hitting the send button. If the user enters the correct frequency of operation in the Frequency box, then each time the slider bar is moved the angle to which the beam will be steered is presented in the Beam Steer Angle box. Also, in the case where the transmit and receive amplifiers are being used, the Mode buttons allow one the direction of the signals to be chosen. The status window displays statements that verify that the interface is working correctly.

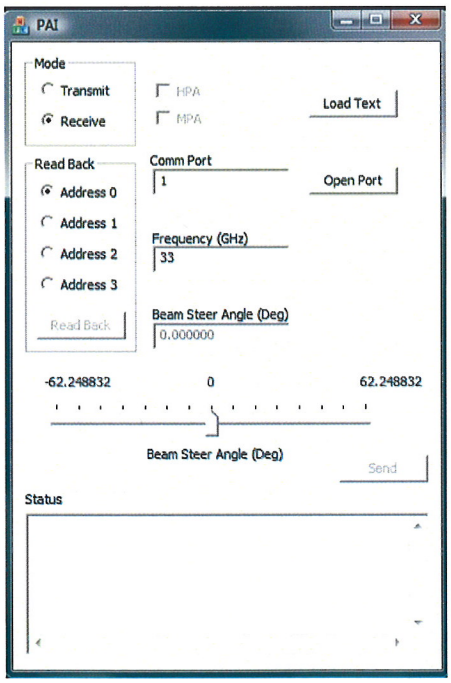


Figure 22. Phased Array Assembly Computer Control Interface

V. TESTING

The testing of the phased array assembly was conducted in two stages, calibration and pattern measurement. The array was first calibrated using a vector network analyzer and RF coplanar probe station. S-parameter data was collected for measurements between the microwave input connector and the output of each phase shifter. This data was collected over a frequency range of 31 to 36 GHz. This data was used to compute the relative phase difference between phase shifter settings across the array. The phase values measured at 33, 33.5, 34, 34.5 and 35 GHz were used to create the look-up tables used by the PAI during the pattern measurements of the array. The look-up tables were created by reading all of the measured data into Matlab and then using a function to find the phase shifter settings that will lead to the closest fit possible to the desired phase slope across the array. Figure 23 shows a plot of how this is done. The x-axis represents each of the 16 phase shifters. The y-axis represents the relative phase measurement in degrees. The different lines represent the 16 different phase settings available by each phase shifter. The legend shows which 4-bit setting was asserted on the phase shifters for each line. The black dashed line overlaying the phase measurements is the ideal line for the desired phase slope. The circles near the ideal line are the phase settings available that most closely fits the ideal phase line. In this figure it is seen that a 22.5-degree slope was solved for.

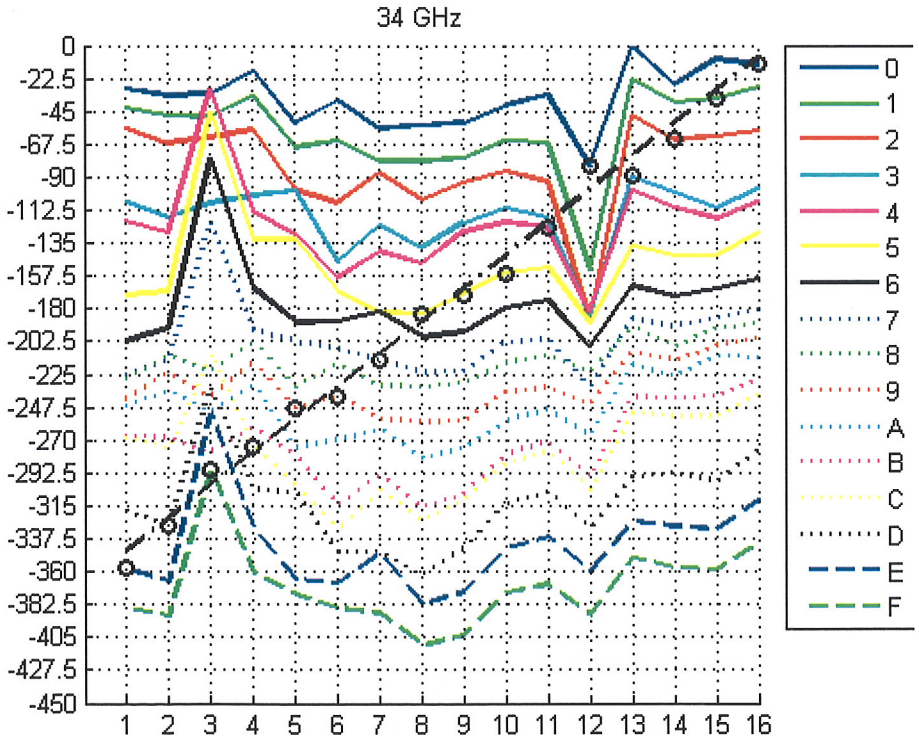


Figure 23. 34GHz Phase Measurements and Phase Setting Solver Example

Figure 23 also shows how well the phase shifters work. They are supposed to have a 22.5-degree phase shift between each bit increment. It is seen that, for the most part, the phase shifters do nearly apply the correct phase steps. However, the phase shifters on channels 3 and 12 appear to have some problems, or stuck bits, as shown by the sharp discontinuities in the data for several of their phase settings. Plots of the phase measurements at 33, 33.5, 34, 34.5, and 35 GHz are included in Appendix A.

The amplitude for each channel was also measured. These measurements will show how well the amplitude was tapered across the array. Figure 24 shows a plot of the relative amplitudes measured for each channel, as well as the ideal case generated from the values shown previously in Table 3. In this plot it is seen that a couple of the channels are slightly off, but for the most part, the amplitudes follow the desired amplitude weighting. This plot was created for measurements made with all of the phase shifters set to the same phase shift. Figure 25 shows the same plot but with the phase shifters set such that the beam is steered using the phase settings solved for and shown in Figure 23. In Figure 25, while the amplitude trend follows the desired weighting, it is seen that significant amplitude errors are occurring. It is believe that these errors are originating from two sources. The first is from the amplitude variation that phase shifters can have between different phase settings.

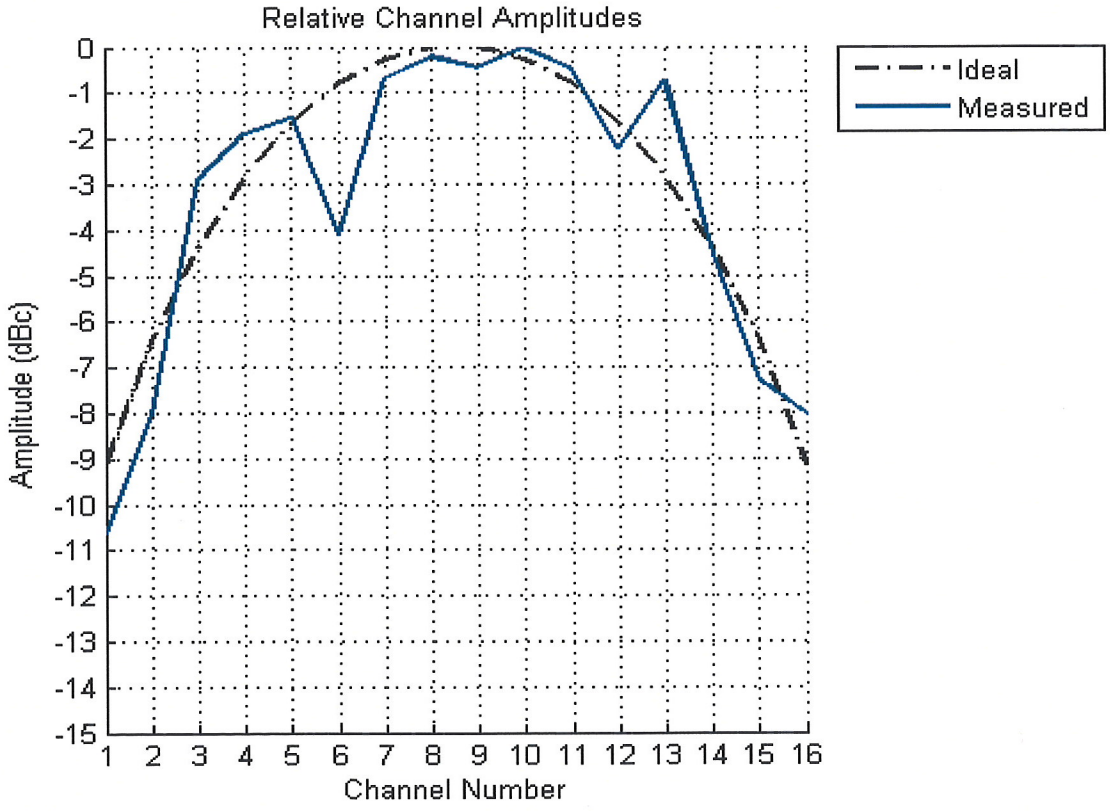


Figure 24. Measured Relative Amplitude Versus Channel Number

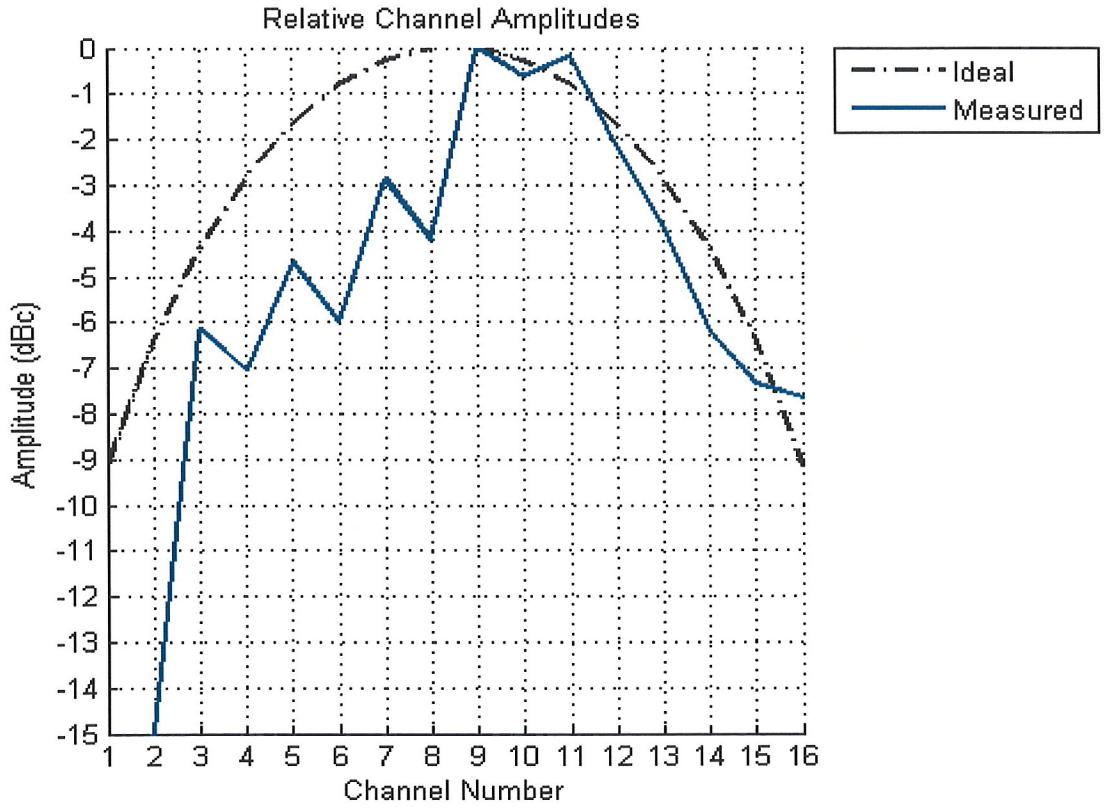


Figure 25. Measured Relative Amplitude Versus Channel Number

The second is from not having enough isolation between the power divider outputs. Poor channel isolation can lead to amplitude and phase errors that vary with phase shifter setting. This can happen if the input return loss of the phase shifters vary with phase setting and the reflected power then ends up in the adjacent channels and corrupts their signal. From other plots similar to Figure 25 it was found that the lower channels, especially channel 6, had the most issues with amplitude fluctuations with changing phase shifter settings. This may not come as a surprise since channel 6 required some rework during the lab testing and debugging phase of this program. Redesigning the power divider using a topology that will lead to more channel isolation may help mitigate errors due to reflections. A method of varying the gain of each channel independently will be required to best remove amplitude errors.

The antenna patterns for the array assembly were measured in the compact range anechoic chamber at Building 5400. The array assembly was mounted to a computer-controlled pedestal for angle scanning. The antenna patterns were measured over a 180-degree span. Pictures of the array assembly and pedestal mount in the compact range are shown in Figures 26 and 27.

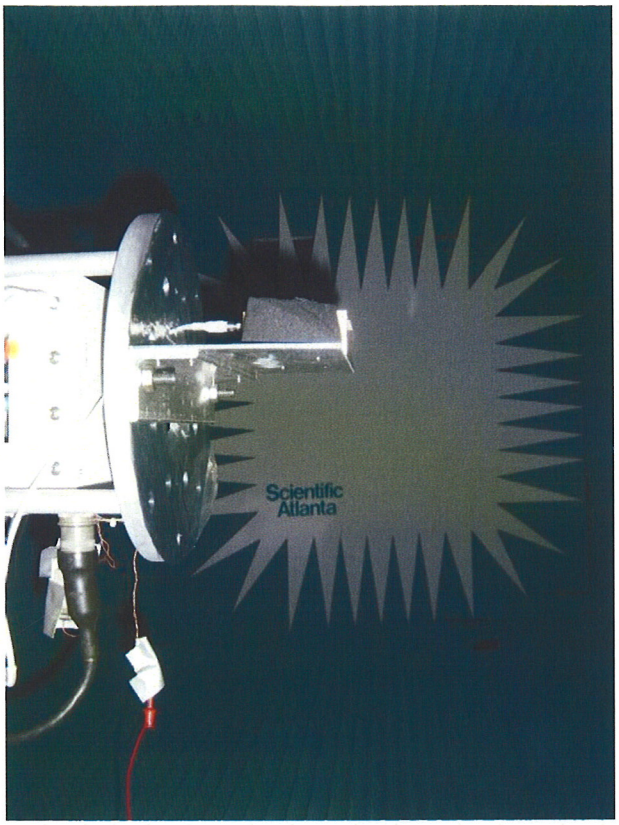


Figure 26. Picture of Compact Range with Array Assembly Pointed in the +90-Degree Direction

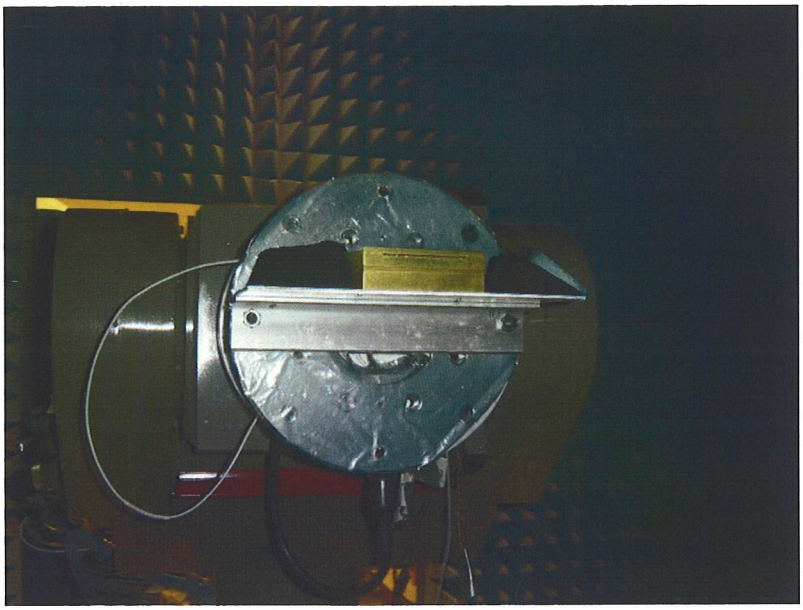


Figure 27. Front of the Array Assembly on the Pedestal

Antenna pattern measurements were made at 33, 33.5, 34, 34.5, and 35 GHz. For each frequency the beam was steered to several angles. Some plots that display some of the better measurements are shown in Figures 28 through 32. The plots of all of the measured data are shown in Appendix B. In the plots shown in Appendix B, it can be seen that the patterns start to break down when steering past 40 degrees. This agrees well with the simulated results of the four-element array.

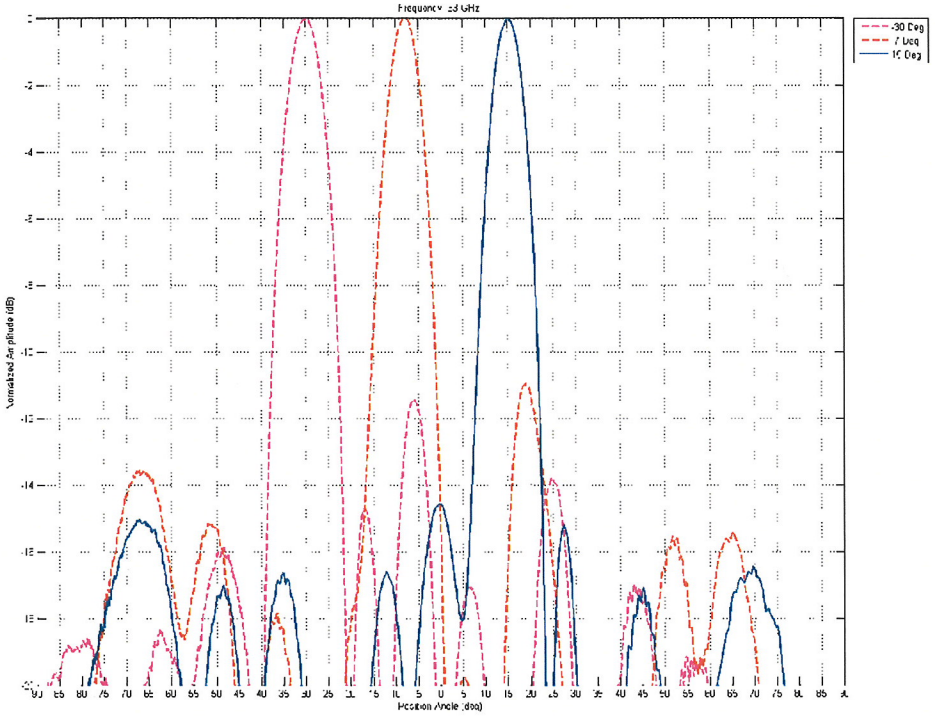


Figure 28. 33 GHz Pattern Measurements

With most of the plots shown here, there are still some noticeable side lobes and main beam deformations. It can be shown that the channel amplitude errors have a more significant effect than phase errors in terms of pattern distortion. Therefore, based on earlier discussions, there may be noticeable channel amplitude errors due to insufficient channel isolation and the varying phase shifter insertion loss. Thus, it can be speculated that the pattern distortion shown in these plots are generated from these amplitude errors.

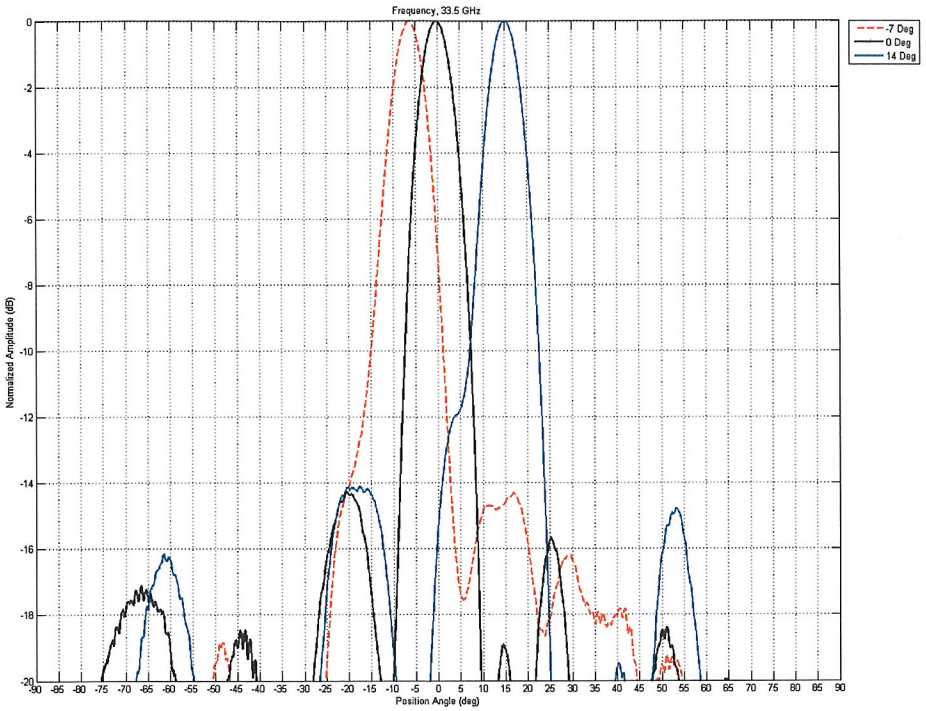


Figure 29. 33.5 GHz Pattern Measurements

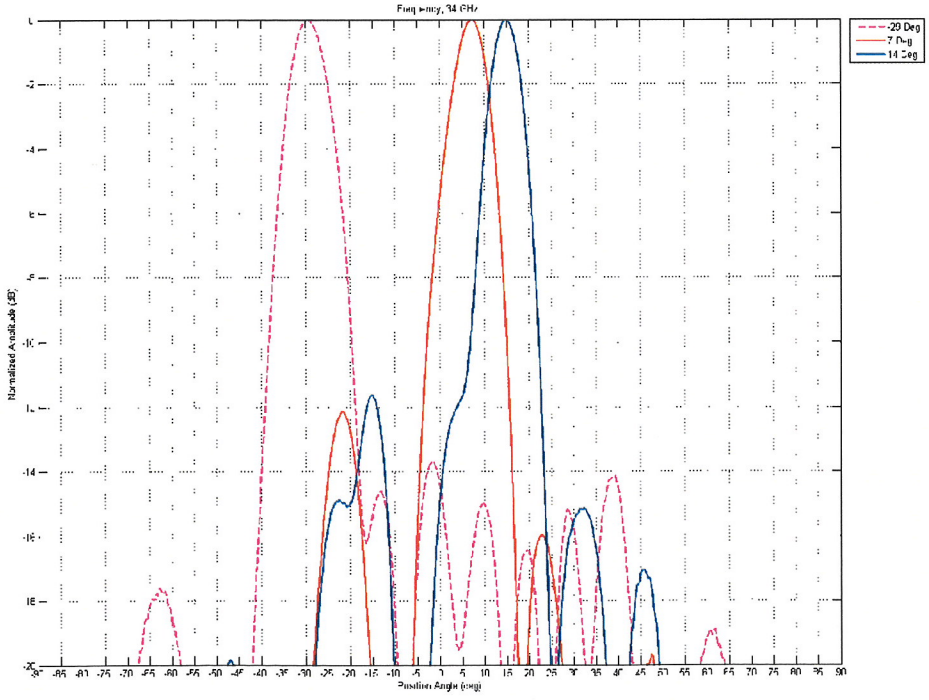


Figure 30. 34 GHz Pattern Measurements

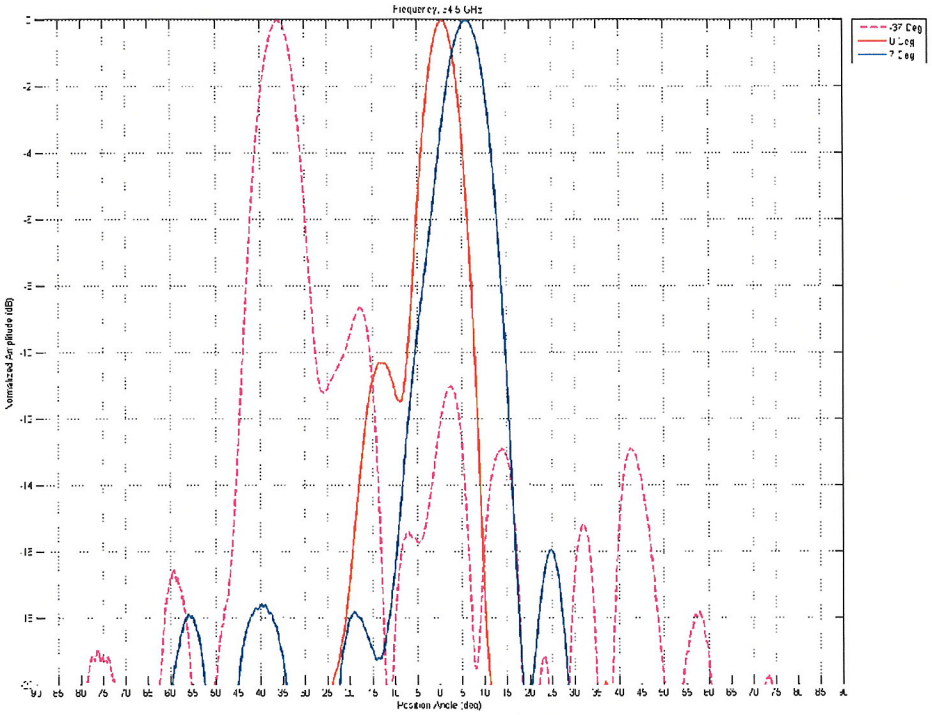


Figure 31. 34.5 GHz Pattern Measurements

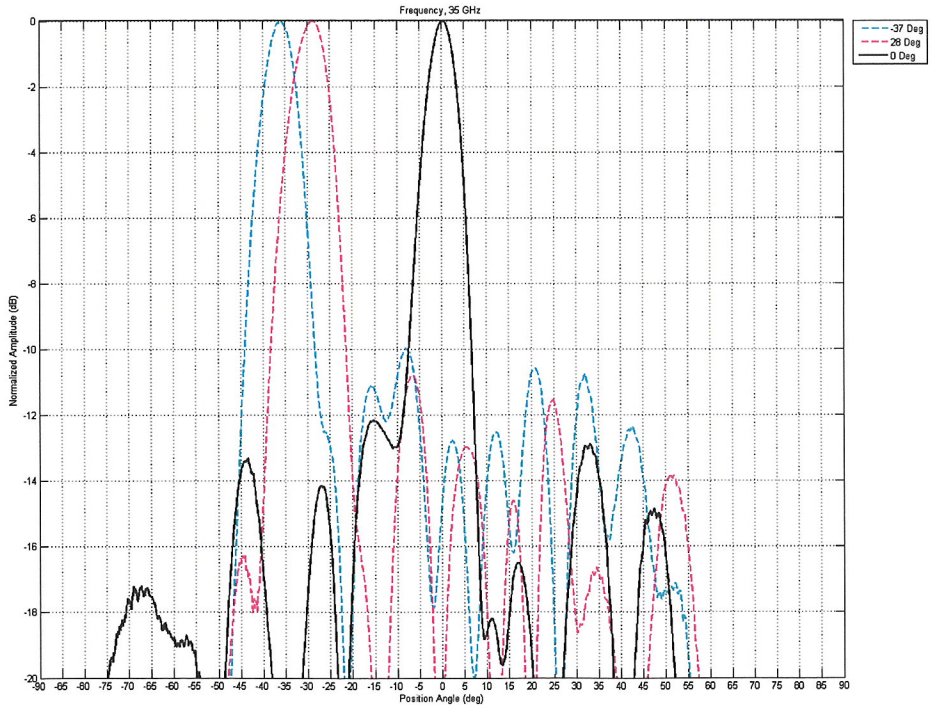


Figure 32. 35 GHz Pattern Measurements

VI. CONCLUSION AND DISCUSSIONS

To our knowledge, this represents the first passive electronically-steerable phased array slat populated with packaged MEMS devices at Ka-band. The Raytheon MEMS-based phase shifters developed under the CERDEC MTO are significantly mature but not the only 4-bit phase shifters known to the Government at Ka-band. They were chosen for this task due to the collaborative environment with CERDEC and AMRDEC.

The Ka-band linear array presented in this report demonstrates the capability to design and fabricate a fully integrated MEMS phase shifter phased array with angle scanning. Additional efforts in the following areas are needed to continue to mature and demonstrate the capabilities of MEMS RF devices:

- There is an interest in redesigning the microwave board. The items that should be considered in a redesign are the power divider, the addition of channel gain control, and the antennas. The power divider could be redesigned to have more channel-to-channel isolation to aid in mitigating amplitude and phase errors due to varying reflections when changing phase shifter settings. The addition of gain control allows one to more accurately control the relative channel amplitudes which would help reduce sidelobe levels. In this program it was found that the antennas themselves were very fragile due to how thin the substrate material was. Minimal effort would be required to develop a more rigid design.
- Another area of future development is the extension of the linear array to two dimensions. At present, the linear array is arranged with elements in a side-by-side configuration. If the other dimension is to be used the elements will be in a stacked configuration and could potentially have different performance in this arrangement. The element patterns will probably not be significantly affected, but there is the possibility of more element coupling (i.e., lower isolation) between stacked elements when compared with the side-by-side linear array. This effect should be investigated to evaluate the scanning performance of the full, 2-D array.

REFERENCES

1. Goldsmith, C.L.; Zhimin Yao; Eshelman, S.; Denniston, D.; "Performance of low-loss RF MEMS Capacitive Switches," Microwave and Guided Wave Letters, IEEE [see also IEEE Microwave and Wireless Components Letters] Volume 8, Issue 8, August 1998 Page(s):269 – 271.

2. Pillans, B.; Morris, F.; Chahal, P.; Frazier, G.; Jeong-Bong Lee; "Schottky Barrier Contact-Based RF MEMS Switch," Micro Electro Mechanical Systems, 2007. MEMS. IEEE 20th International Conference on 21-25 Jan. 2007 Page(s):167 - 170IMS 2007 – Honolulu, Hawaii.

3. "Near Hermetic Wafer Level Packaging Using LCP Adhesive Layer," Cody Moody, Brandon Pillans, Andrew Malczewski, and Francis J. Morris, IMAPS International Conference on Device Packaging, Scottsdale/Fountain Hills, AZ (9-12 March 2009) WP26.

4. Pillans, B.; Coryell, L.; Malczewski, A.; Moody, C.; Morris, F.; Pillai, V.; "RF MEMS Phase Shifter Manufacturing Technology," Defense Manufacturing Conference 2008, Orlando, FL.

5. Atwater, Harry A., "Circuit Design of the Loaded-Line Phase Shifter," *IEEE Transactions on Microwave Theory and Techniques*, Vol. MTT-33, No. 7, July 1985, pp. 626-634.

6. Opp, Francis L. and Hoffman, W. F., "Design of Digital Loaded-Line Phase-Shift Networks for Microwave Thin-Film Applications," *IEEE Transactions on Microwave Theory and Techniques*, Vol. MTT-16, No. 7, July 1968, pp. 462-468.

7. Rebeiz, Gabriel M., RF MEMS, Theory, Design, and Technology, John Wiley & Sons, Inc., New Jersey, 2003, pp. 221-257.

8. P. J. Gibson, "The Vivaldi Aerial," in *Proc. 9th Eur. Microwave Conf.*, Brighton, U.K., Sept.. 1979, pp. 101–105.

9. E. Gazit, "Improved Design of the Vivaldi Antenna," *IEE Proc., Part H*, Vol. 135, No. 2, 1988, pp. 89–92.

10. S. G. Kim and K. Chang, "A Low Cross-Polarized Antipodal Vivaldi Antenna Array for Wide-Band Operation," in *Proc. IEEE Int. AP-S Symp.*, Monterey, CA, Jun. 2004, pp. 2269–2272.

APPENDIX A
PHASE MEASUREMENT

Appendix A

Phase Measurements

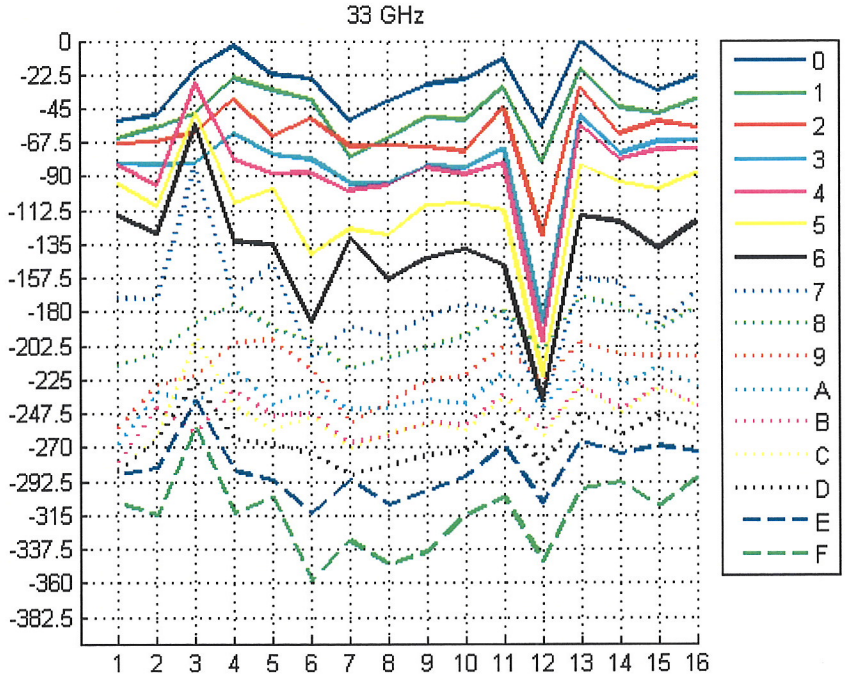


Figure A-1. 33 GHz Phase Measurements vs Channel Number for Each Phase Shifter Setting

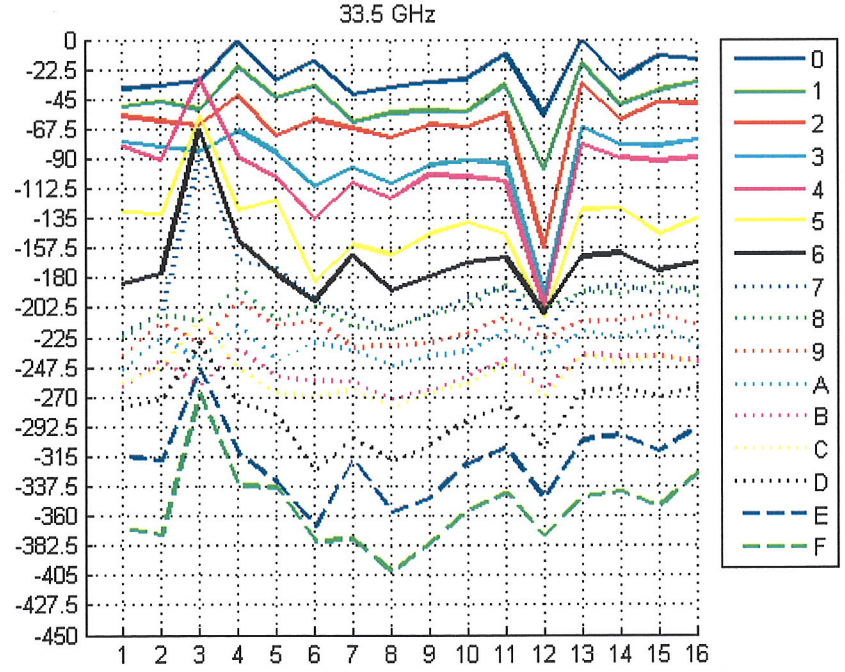


Figure A-2. 33.5 GHz Phase Measurements vs Channel Number for Each Phase Shifter Setting

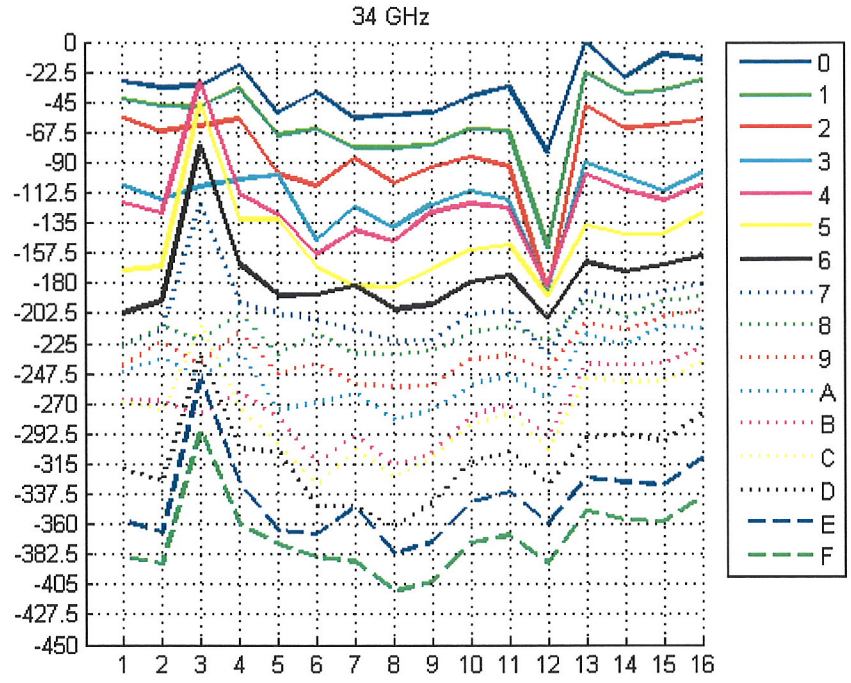


Figure A-3. 34 GHz Phase Measurements vs Channel Number for Each Phase Shifter Setting

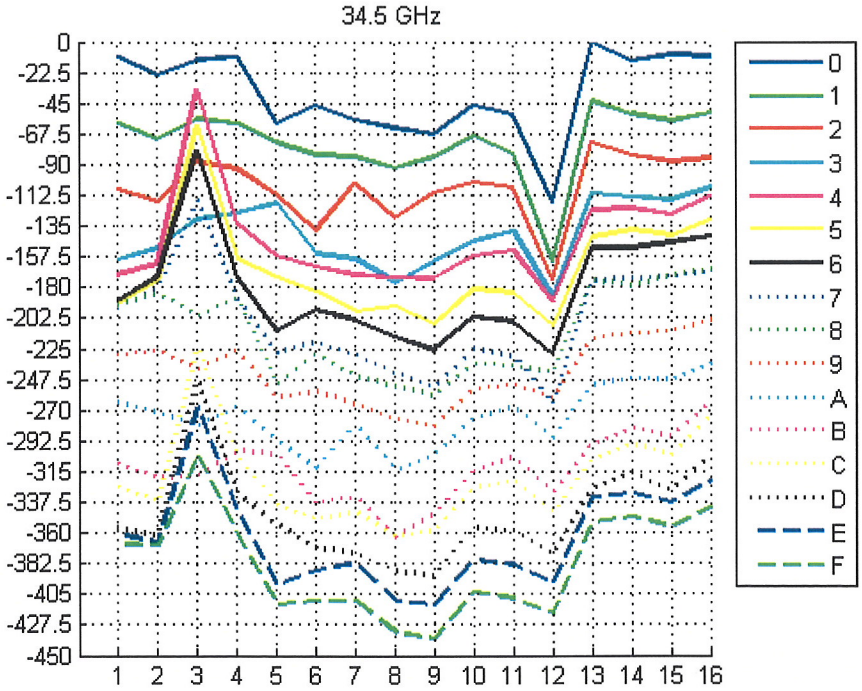


Figure A-4. 34.5 GHz Phase Measurements vs Channel Number for Each Phase Shifter Setting

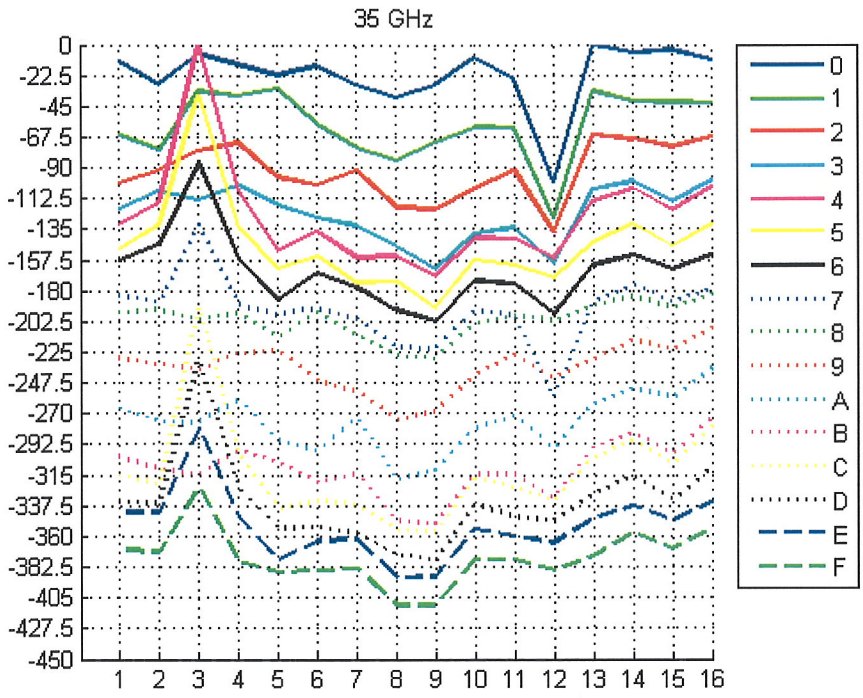


Figure A-5. 35 GHz Phase Measurements vs Channel Number for Each Phase Shifter Setting

APPENDIX B
PATTERN MEASUREMENTS

Appendix B

Pattern Measurements

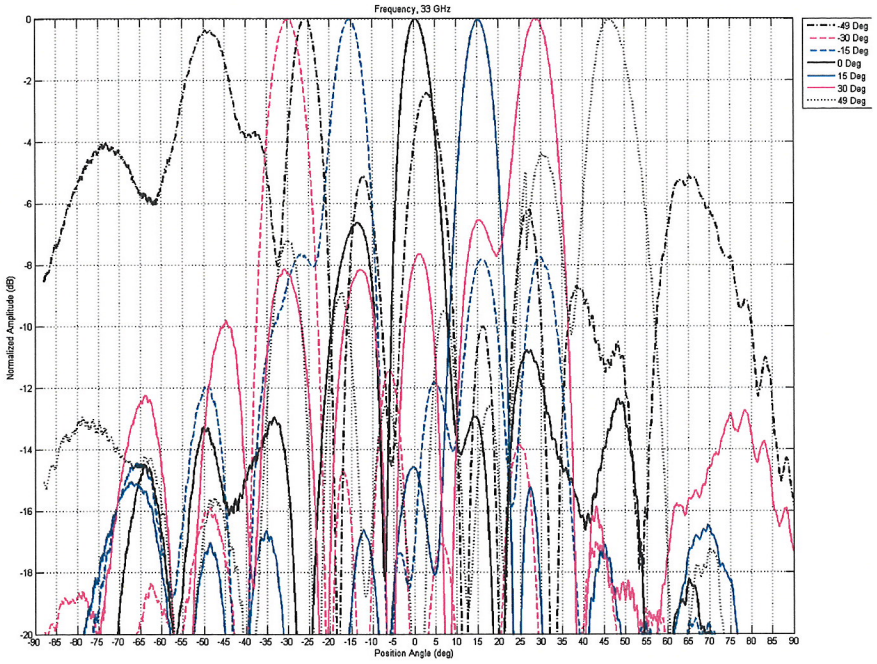


Figure B-1. 33 GHz Pattern Measurements Plot 1

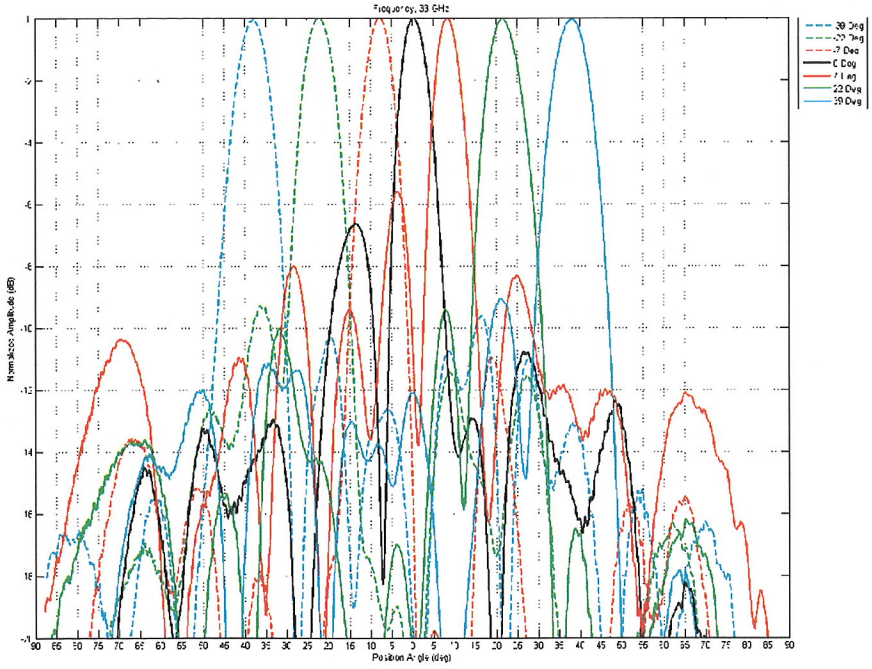


Figure B-2. 33 GHz Pattern Measurements Plot 2

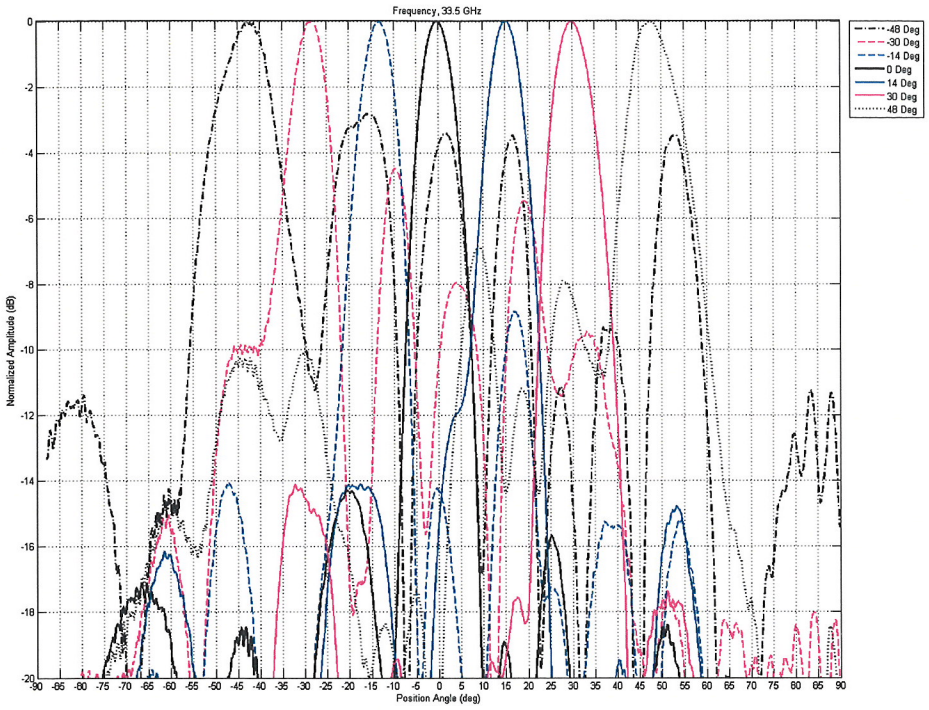


Figure B-3. 33.5 GHz Pattern Measurements

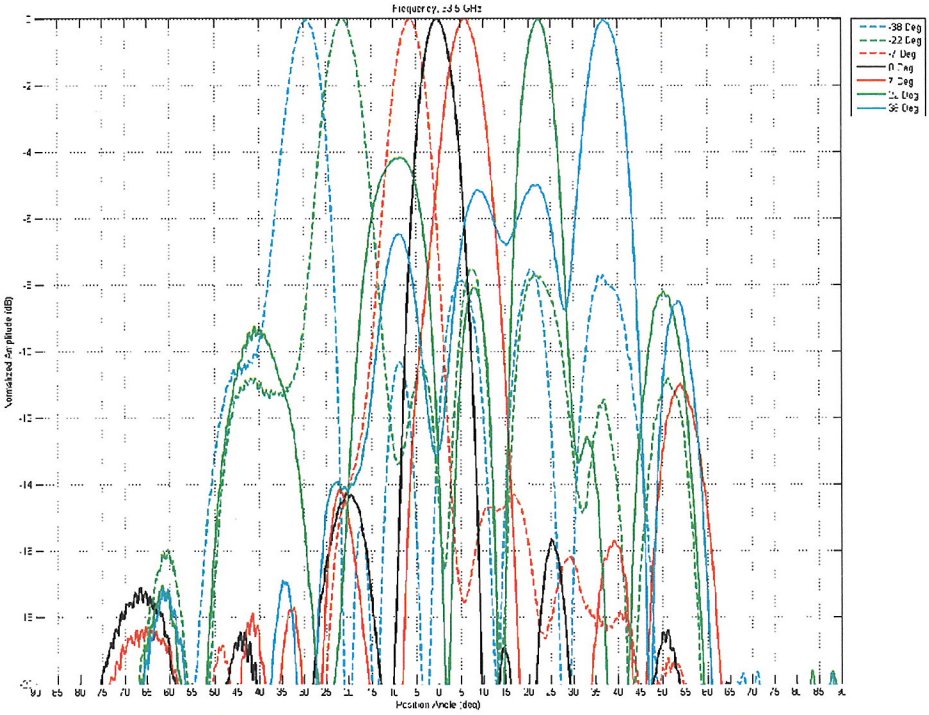


Figure B-4. 33.5 GHz Pattern Measurements

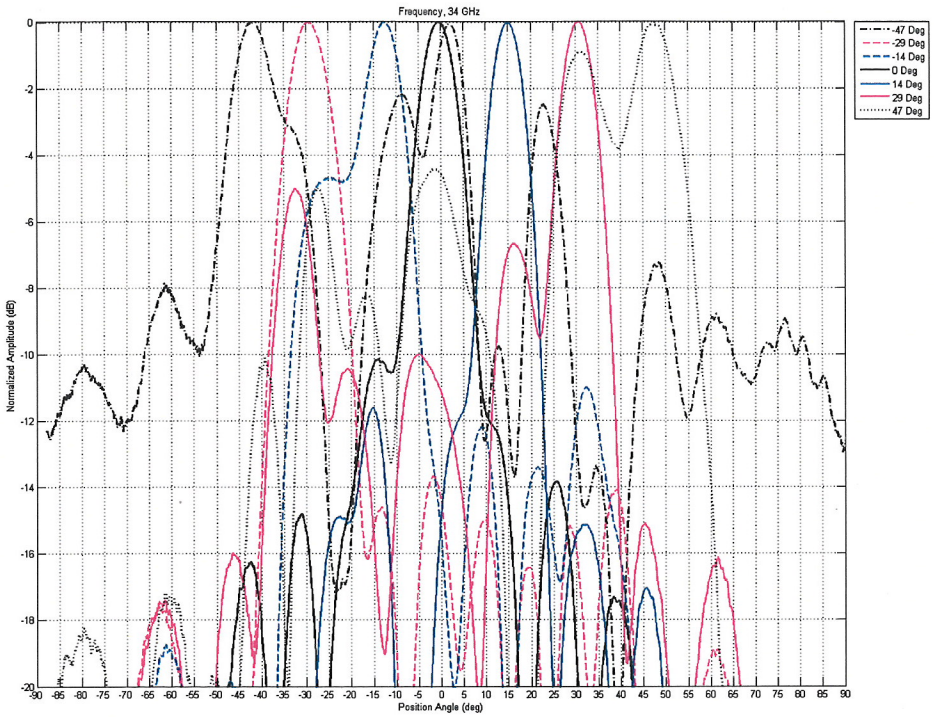


Figure B-5. 34 GHz Pattern Measurements

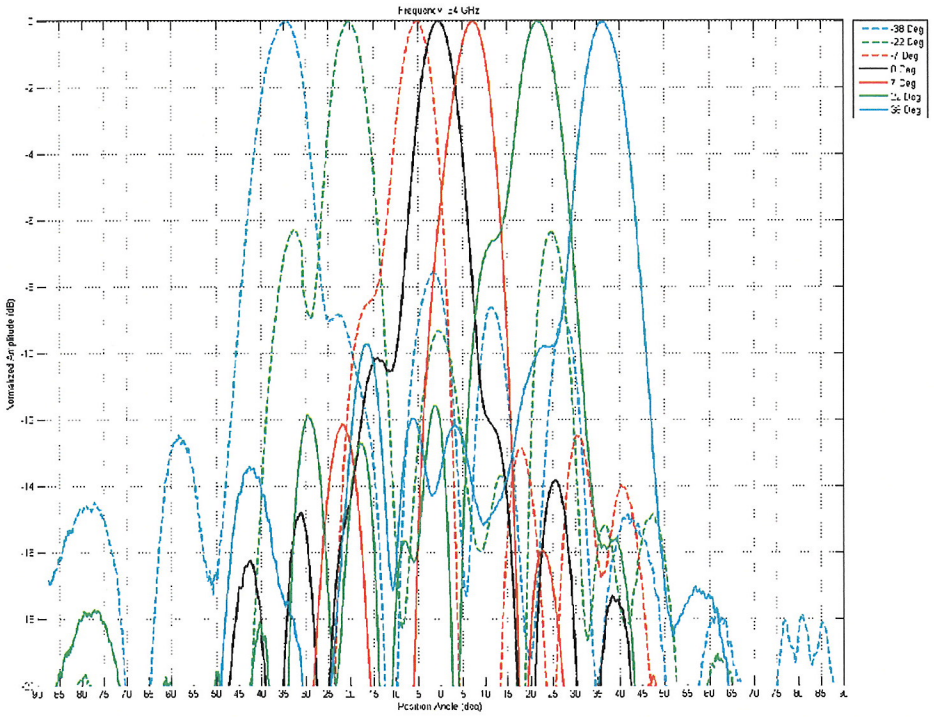


Figure B-6. 34 GHz Pattern Measurements

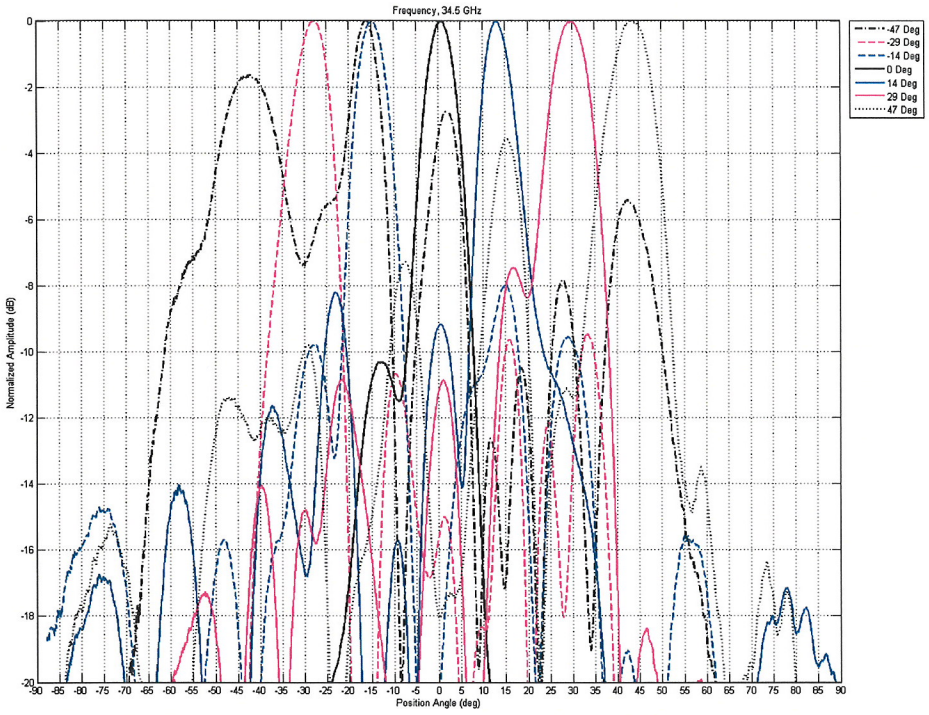


Figure B-7. 34.5 GHz Pattern Measurements

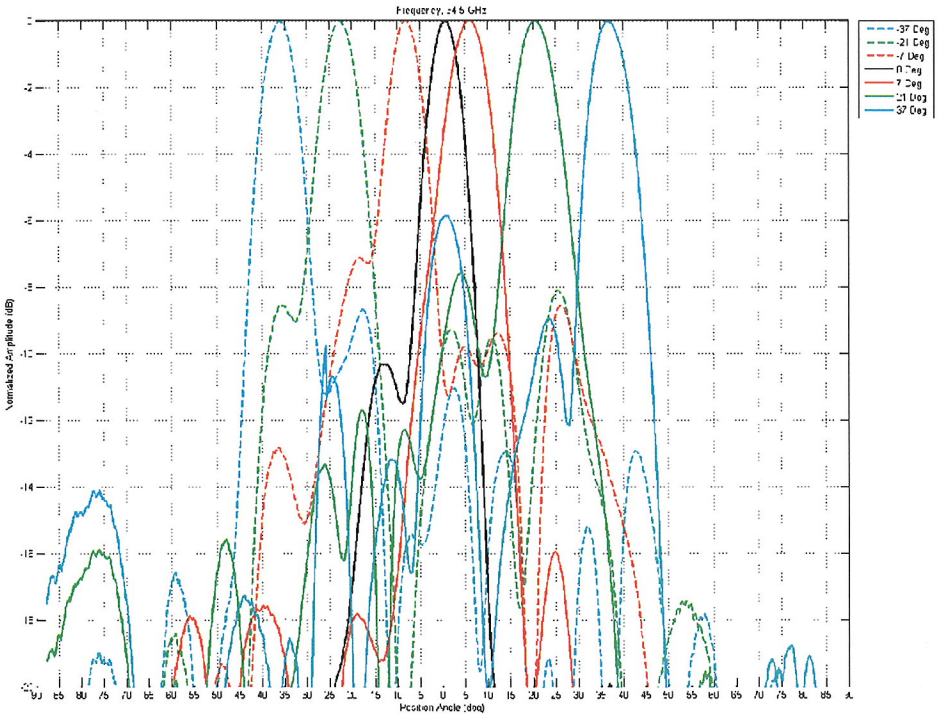


Figure B-8. 34.5 GHz Pattern Measurements

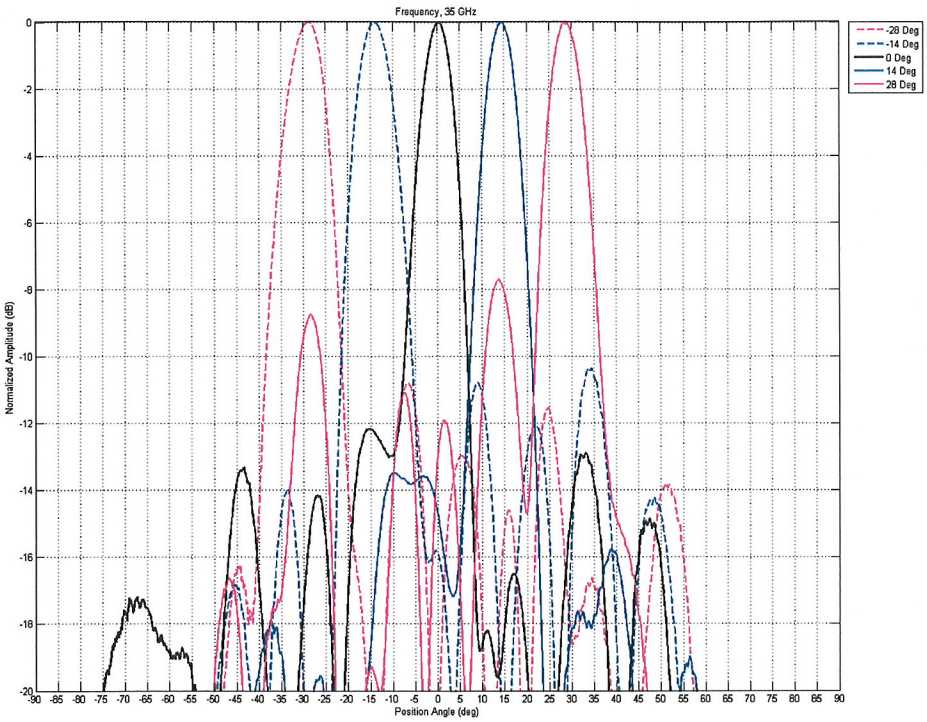


Figure B-9. 35 GHz Pattern Measurements

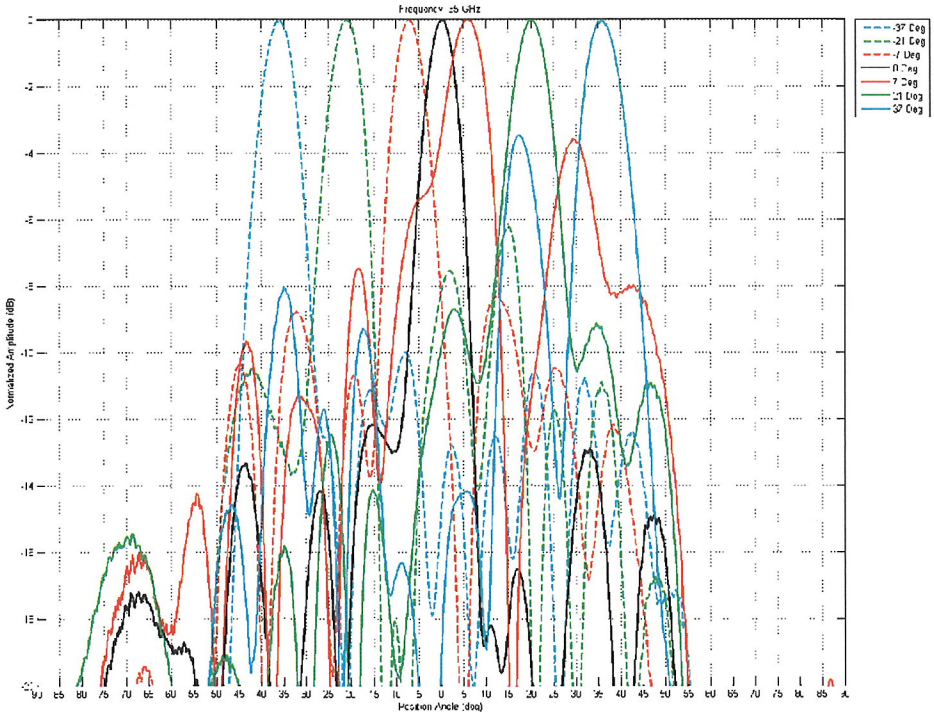


Figure B-10. 35 GHz Pattern Measurements

INITIAL DISTRIBUTION LIST

		Copies
Weapon Systems Technology Information Analysis Center Alion Science and Technology 201 Mill Street Rome, NY 13440	Ms. Perry E. Onderdonk ponderdonk@alionscience.com	Electronic
Defense Technical Information Center 8725 John J. Kingman Rd., Suite 0944 Fort Belvoir, VA 22060-6218	Mr. Jack L. Rike jrike@dtic.mil	Electronic
AMSRD-CER-ST-SS-TS,	Mr. Louis A. Coryell Louis.coryell@us.army.mil	Electronic
AMSRD-L-G-I,	Ms. Anne C. Lanteigne anne.lanteigne@us.army.mil	Electronic
RDMR		Electronic
RDMR-CSI		Electronic
RDMR-WD,	Dr. Robin B. Buckelew Robin.Buckelew@us.army.mil	Electronic
RDMR-WDS-T,	Mr. Ronald G. Schmalbach Ron.Schmalbach@us.army.mil	Electronic
RDMR-WD,	Mr. James E. Hatfield, III Jim.Hatfield@us.army.mil	Electronic
RDMR-WDG-C,	Mr. Roger P. Berry roger.berry@us.army.mil	Electronic
RDMR-WDG-R,	Mr. Joel P. Booth Joel.Booth@us.army.mil	Electronic
	Mr. Christopher A. Harmer Chris.Hamner@us.army.mil	Electronic
	Mr. Randy R. McElroy Randy.R.McElroy@us.army.mil	Electronic
	Mr. James H. Mullins, III James.Mullinsiii@us.army.mil	Electronic
	Ms. Janice C. Rock Janice.Rock@us.army.mil	Electronic Hard Copy
	Dr. Brian J. Smith Brian.Jennings.Smith@us.army.mil	Electronic

INITIAL DISTRIBUTION LIST (CONTINUED)

		Copies
RDMR-WDS-S,	Dr. James L. Baumann james.baumann1@us.army.mil	Electronic
	Mr. R. William Nourse Bill.Nourse@us.army.mil	Electronic
	Mr. Heinz G. Sage Heinz.Sage@us.army.mil	Electronic
RDMR--WDR,	Dr. Paul B. Ruffin Paul.Ruffin@us.army.mil	Electronic
RDMR--WDP-S,	Mr. Jason C. Gilliam Jason.Gilliam1@us.army.mil	Electronic
A. Brown Design 46055 Bloomcrest Drive Northville, MI 48167	Mr. Andrew R. Brown Andrew.r.brown@sbcglobal.net	Electronic
Dynetics, Inc. 1002 Explorer Boulevard Huntsville, AL 35806	Mr. Richard A. Milburn Richard.milburn@dynetics.com	Electronic
Phase IV Systems Operation 3405 Triana Boulevard Huntsville, AL 35805	Dr. Daniel E. Lawrence Dan.lawrence@phaseiv.com	Electronic
	Mr. Brandon J. Wolfson brandon.wolfson@phaseiv.com	Electronic
Raytheon Space and Airborne Systems Advanced Products Center Dallas, TX 75243	Dr. Brandon W. Pillans b-pillans@raytheon.com	Electronic